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Broad Bandwidth High Resolution Analog to Digital Converters: Theory, Architecture and Implementation

Saiyu Ren
Wright State University

BROAD BANDWIDTH HIGH RESOLUTION ANALOG TO DIGITAL CONVERTERS: THEORY, ARCHITECTURE AND IMPLEMENTATION

A dissertation submitted in partial fulfillment of the
Requirements for a degree of
Doctor of Philosophy

By

SAIYU REN
B.S Electrical Engineering, South China University of Technologies, 1985
M.S., Institute of Semiconductor, Chinese Academy of Sciences, 1988
M.S. Engineering, Wright State University, 2001

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WRIGHT STATE UNIVERSITY

SCHOOL OF GRADUATE STUDIES

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I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Saiyu Ren ENTITLED Broad Bandwidth High Resolution Analog to Digital Converters: Theory, Architecture and Implementation BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

_____

Raymond Siferd, Ph.D.
Dissertation Director

_____

Ramana V. Grandhi, Ph.D.
Director, Engineering Ph.D. Program

_____

Joseph F. Thomas, Jr., Ph.D
Dean, School of Graduate Studies

Committee on
Final Examination

_____
Raymond E. Siferd, Ph.D.

_____
Henry Chen, Ph.D.

_____
Marian K. Kazimierczuk, Ph.D.

_____
John M. Emmert, Ph.D.

_____
Frank Scarpino, Ph.D.

ABSTRACT

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Analog to digital converters (ADCs) translate analog quantities, which are characteristic of most phenomena in the "real world" to digital language for a variety of applications including information processing, computing, communication and control systems. The performance of the digital signal processing and communication systems is generally limited by the speed and precision of the digital input signal which is achieved at the interface between analog and digital information. The analog to digital converter (ADC) has become a critical component for advanced telecommunication systems. The desire to move the analog to digital interface closer to the sensor has resulted in more stringent performance requirements for high speed, and high resolution ADCs. High speed ADCs have become the bottle neck for achieving high performance signal processing systems. This has motivated many researchers and scientists to continuously work on the development of innovative ADC architectures and new techniques.

The dissertation is going to present

1) The design, fabrication and testing for a CMOS ADC architecture which has up to 62.5 MHz base bandwidth and 1 GHz sample frequency with 12 bits resolution. This work is done by using a unique patented architecture, "Pipelined Delta Sigma Modulator Analog to Digital Converter".

2) A CMOS band pass ADC which includes M single channel sub-sampling delta sigma modulators having N-bit quantizer outputs arranged in a time interleaved

configuration. This unique patented architecture facilitates a flexible RF/IF Band Pass ADC. MATLAB SIMULINK simulation results show that more than 8 bits of resolution are obtained for center frequencies in the 1.8 GHz to 3.0 GHz region with a bandwidth of 70 MHz using time interleaved first order delta sigma modulators operating with sampling frequencies of 600 MHz to 1.0 GHz.

3) The design, fabrication and testing for CMOS Phase Lock Loop synthesizer architectures which will be able to generate In phase and Quadrature clock signals up to 7.8GHz frequency which may be used as the ADCs and receivers on chip clock source.

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1 Introduction

Analog to digital converters (ADCs) translate analog quantities which are characteristic of most phenomena in the "real world" to digital language for a variety of applications including information processing, computing, communication and control systems. The performance of the digital signal processing and communication systems is generally limited by the speed and precision of the digital input signal which is achieved at the interface between analog and digital information. The analog to digital converter (ADC) has become a critical component for advanced telecommunication systems. The desire to move the analog to digital interface closer to the sensor has resulted in more stringent performance requirements for high speed, high resolution ADCs. High speed ADCs are the essential part of the signal processing and becomes the bottle neck of the signal processing system. This attracts many researchers and scientists to develop some innovated ADC architectures and even new techniques.

1.1 Review of Some Basic Concepts

1. Sample Rate

A continuous analog signal is sampled at discrete time interval, ts=1/fs, where fs is called sampling frequency, sampling rate or sample rate. The sampling theorem states that for a limited bandwidth (band-limited) signal with maximum frequency fmax, the equally spaced sampling frequency fs must be greater than twice of the maximum frequency fmax in order to have the signal be uniquely reconstructed without aliasing. This sampling theorem was set forth by Nyquist in 1928 [1,2] and mathematically proven by Shannon in 1948 [3]. It is clear that the more sample taken, the more accurate the digital

representation and easier to recover the original signal from the sampled signal. The sampling at more than twice the bandwidth is called over sampling. Sampling at less than twice the bandwidth is called undersampling or subsampling which results in aliasing or imaging of the signal. The frequency domain is shown in Figure 1.1[4] which is divided into an infinite number of Nyquist zones, each having a width equal to 0.5fs. From DC to 0.5fs is called 1st Nyquist zone; 0.5fs to fs is called the 2nd Nyquist zone; and so on. If fs is more than twice of fa (fa is the input signal frequency), all the frequencies of interest lie within the 1st Nyquist zone with images on fs-fa, fs+fa, 2fs-fa, 2fs+fa, … |±Kfs±fa|, K=1, 2, … as seen the top figure of Figure 1.1. All the images will be filtered out by the low pass filter. If fs is less than twice of fa, the signal will be on the higher Nyquist zone. For example, if 0.5fs < fa <fs, the signal which labeled as fa lies in the 2nd Nyquist zone, and images which labeled as I will be on the 1st, 3rd and 4th, … Nyquist zones as seen the bottom figure of Figure 1.1. The images on the 1st Nyquist zone has all the information of the original signal which can be used to restore the original signal by the sampled signal with the proper time control sequence which will be discussed later. This technique can be used for high bandwidth applications without increasing the sample frequency.

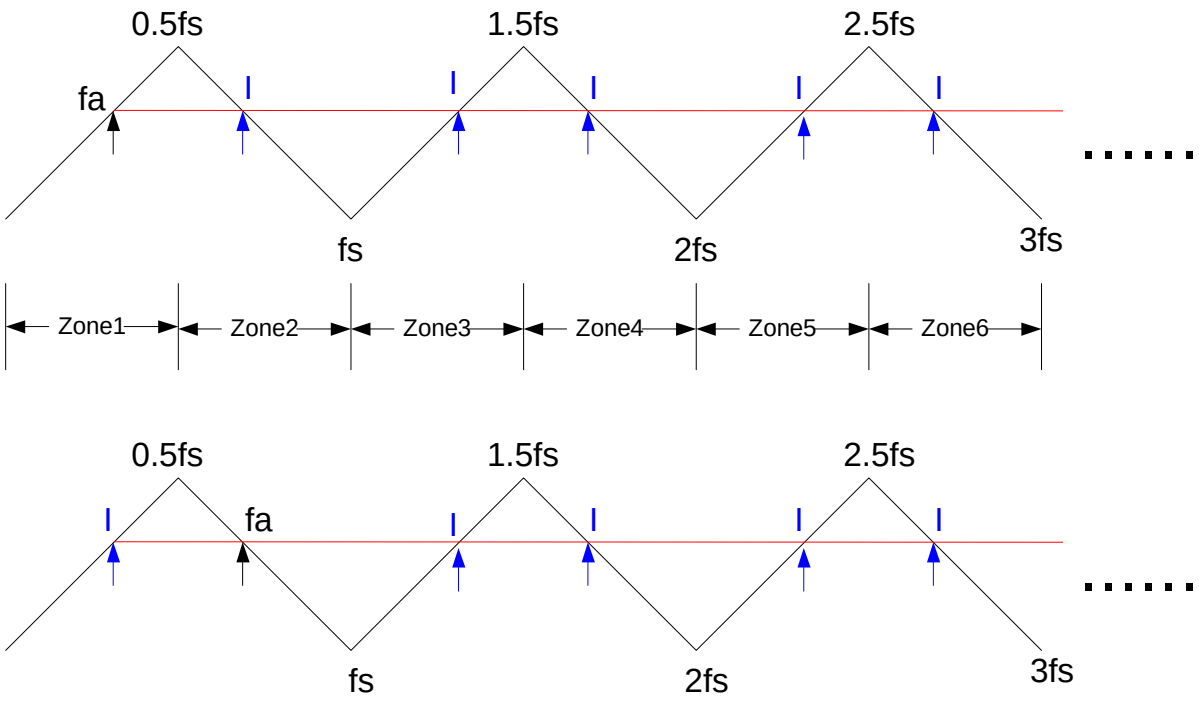

Figure 1.1 Sample Rate Definition Chart

2. Quantization Error (Noise)

Quantization is the procedure of constraining an analog signal to a discrete set of values which are represented by a group of digital values. The difference of every two consecutive digital values is one LSB (Least Significant Bit). The value of LSB can be defined as

$$LSB = \frac{V_{REFP} - V_{REFN}}{2^N} = \frac{FSR}{2^N} \qquad \textbf{(1.1)}$$

Where N is the number of quantization bits; V_{REFP} is the positive reference voltage and V_{REFN} is the negative reference voltage; FSR is the Full Scale Range.

Quantization error is the difference between the signal analog value and its digitized value. It is usually modeled as the rms quantization noise to quantify the error. The rms quantization noise is expressed as below [5].

$$\text{rms(quantization noise)} = \frac{\text{LSB}}{\sqrt{12}} = \frac{FSR}{2^N \sqrt{12}} \quad \textbf{(1.2)}$$

3. Phase Noise

The term phase noise is used to describe phase fluctuations due to the random frequency fluctuations of a signal. Phase noise can be caused by a number of conditions, but is mostly affected by oscillator frequency stability [6]. The measurement of the phase noise is based on oscillators tending to amplify any noise near the oscillation frequency; the closer the noise frequency to the oscillation frequency, the greater the amplification is. Phase noise is centered about the oscillation frequency, so filtering can never completely remove it. Phase noise is typically expressed in units of dBc/Hz at various offsets from the carrier frequency. dBc means "in dB with respect to carrier". Assume the carrier power is Pc dBm, and a unit bandwidth noise power at an offset $\Delta\omega$ with relative to carrier frequency ω_c is Pn dBm. Then the phase noise is (Pn-Pc) dBc/Hz. If the noise power is measured in a fb bandwidth, then the phase noise will be calculated as (Pn-Pc-10log(fb)) dBc/Hz [7].

4. Phase Noise Contribution to Jitter

The quality of a clock is usually described by phase noise or jitter measurement. Period jitter (J_{PER}) is the most popular used jitter measurement which is defined as the time difference between a measured cycle period and the ideal cycle period. The period to period jitter due to the phase noise can be calculated as [8]

$$\sigma_\tau = \frac{1}{f_0^{1.5}} 10^{L(f)/20} \tag{1.3}$$

where f is the offset frequency from the clock frequency, and it has to be in the region where the phase noise decreases 20dB per decade; L(f) is the phase noise at the offset frequency; f0 is the carrier frequency.

5. Analog Input Bandwidth (BW)

The analog input frequency at which the power of the fundamental frequency is reduced by a specific amount from the peak response. Depending on the manufacturer, this amount is either 1dB or 3dB.

6. FFT (Fast Fourier Transform)

FFT is a fast version of DFT (Discrete Fourier Transform) which reduces the number of computations needed for Npoints from $2N^2$ to $2N\lg N$ [9]. The DFT uses the discrete time domain signal (N points) and transforms that signal to discrete frequency domain representation; so that we would be able to analyze the signal and noises in the frequency domain.

7. Signal-to-Noise Ratio (SNR)

SNR is a measure of signal strength relative to background noise, which is defined as the ratio of the fundamental frequency power to the sum of the power of all other spectral components excluding the first nine largest spurs and dc.

$$SNR = 10LOG_{10}\left(\frac{P_{Signal}}{\sum P_{Noise}}\right) \tag{1.4}$$

8. Signal-to-Noise-And-Distortion (SINAD)

SINAD is the ratio of the fundamental frequency power to the sum of the power of all other spectral components excluding dc.

$$SINAD = 10LOG_{10}\left(\frac{P_{Signal}}{\sum (P_{Distortion} + P_{Noise})}\right) \quad \textbf{(1.5)}$$

9. Effective Number of Bits (ENOB)

ENOB is an indication of the quality of an analog-to-digital converter (ADC), which gives the conversion bit of an ADC. ENOB is defined as below.

$$ENOB = \frac{\left[10LOG_{10}\left(\frac{P_{Full\ Scale}}{\sum (P_{Distortion} + P_{Noise})}\right) - 1.76\right]}{6.02} \quad \textbf{(1.6)}$$

$$ENOB_{SINAD} = \frac{SINAD - 1.76}{6.02} \quad \textbf{(1.7)}$$

$$ENOB_{SNR} = \frac{SNR - 1.76}{6.02} \quad \textbf{(1.8)}$$

10. Spur-Free Dynamic Range (SFDR)

Spur free dynamic range is the ratio of the power of the fundamental frequency to the largest spur whether harmonically related or not. It can be calculated as below:

$$\text{SFDR} = \text{Signal (db)} - \text{Largest Spur (db)} \quad \textbf{(1.9)}$$

1.2 ADC Architecture Review

The following will briefly discuss the most popular ADC architectures.

1.2.1 Flash ADC

Flash ADC architecture, which is also called parallel ADC, is typically the fastest ADC architecture as shown in Figure 1.2 [10]. This architecture requires 2^n-1 comparators and 2^n equal resistors to provide a unique reference voltage to each comparator for an n bit ADC. The reference voltage for each comparator is one least significant bit (LSB) greater than the one below it. The output of each comparator, which is digitized with '0' if the analog input is less than the compared reference voltage and '1' if the analog input voltage is greater than the compared reference voltage, is connected to the digital thermometer code circuit to generate the right coding outputs. The thermometer code outputs will have to be changed to binary digital outputs through the decoder. For example, a 4 bit flash ADC would require 15 comparators, 16 equal resistors; every two consecutive reference voltages are separated by $\Delta V = \frac{(REF+)-(REF-)}{2^4} = LSB$. It generates 15 thermometer coding outputs and 4 bit binary digital outputs. It can be seen that to reach the n bit conversion resolution, both comparators and resistors have to be at least one LSB accurate. The accuracy of the conversion is limited by component matching (comparators and resistors). The more comparators and resistors are used, the harder to keep them matched. As the fastest converter architecture, flash ADCs are suitable for wide bandwidths application but relatively low resolution which is only up to about 8-bit with some correction techniques [11] [12].

As shown in Figure 1.2, a typical flash ADC consumes a lot of power because the large amount of required components which double for every one bit resolution improvement. This can be quite expensive and limits its application, so reducing the power consumption

has been a big issue for flash ADCs application. Two popular techniques to reduce the power increase of flash ADC are analog pre-processing techniques and voltage averaging techniques. Analog pre-processing techniques, which are interpolating (voltage/current), folding techniques, reduces the input-capacitance of the flash ADC and the number of preamplifiers [13,14,15,16]. Averaging is a technique which reduces the offset specification for high speed ADC without requiring larger transistors area. This technique is limited to flash architecture by taking the average value of neighboring node-voltages and thereby reducing the offset demand [17]. The modified averaging technique is interpolation averaging to obviate the need for a large number of comparators or inter-stage digital-analog converters and residual amplifiers [13,14,15, 16].

Other techniques for reducing the power dissipation of flash architecture are using MOS current mode threshold logic gates which obtain a compact encoder circuit to reduce the number of transistors [18] and using an inverter as a comparator along with an NMOS and a PMOS as switches [19].

In summary, the flash ADC is the simplest and fastest ADC with relatively low resolution and high power dissipation. This limits some of its applications. Many innovative architectures have been developed to compensate for the flash ADCs weakness.

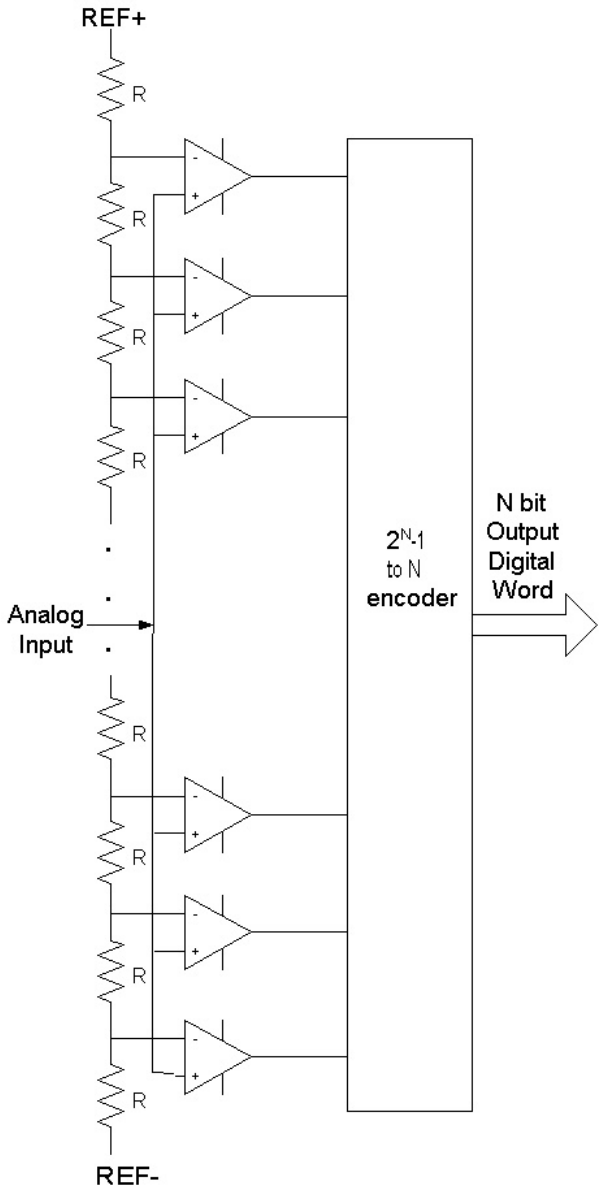

Figure 1.2 All-Parallel (Flash) Converter Architecture

1.2.2 Successive Approximation ADC

The basic successive approximation ADC which is also called Successive Approximation Register ADC (SAR ADC) differs from the flash ADC in that it has only one comparator, one DAC and one control logic and one sample hold circuit as shown in Figure 1.3 [20].

In order to process ac signals, SAR ADCs must have an input sample-and-hold (SHA) to keep the signal constant during the conversion cycle.

The conversion algorithm is similar to the binary search algorithm. At the beginning of the conversion, the internal DAC is set to mid-scale which means that all digital bits are reset to '0' except the most significant bit which is set to '1'. The comparator compares the sample hold signal which keeps in the hold mode with the DAC analog output signal. If the SHA output is above the DAC output, the comparator will output '1' which goes to the control logic to control the result. The most significant bit with '1' will be stored in the successive approximation register (SAR). If the SHA output is below the DAC output, the comparator will output '0'. The most significant bit (MSB) with '0' will be stored in the successive approximation register (SAR). The DAC is then set either to ¼ scale if the MSB is '0' or ¾ scale if the MSB is '1'. The comparator will repeat the comparison and make the decision for next bit after the MSB of the conversion. The result is stored in the register too, and the process continues until all of the bit values have been determined. When all the bits have been set, tested, and reset as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit "tests" form the basis of a serial output version SAR-based ADC.

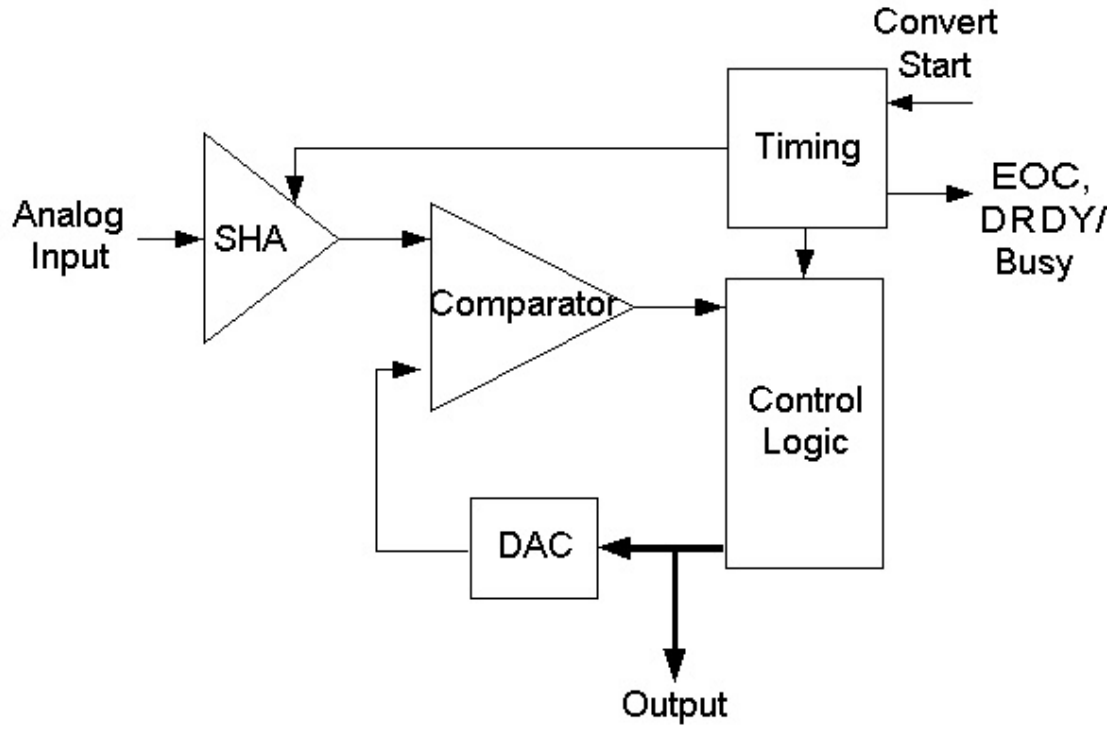

Figure 1.3 Basic SAR Architecture

From the SAR ADC process, it can be seen that the circuit is simple and the power can be reduced a lot compared to the flash architecture. The SAR ADC resolution depends on the resolution of the DAC, which results in much research focusing on the improvement of the DAC resolution. One of the most well known technique is using laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging [20]. Another practical technique is switched capacitor (or charge-redistribution) DAC [21] whose accuracy and linearity is primarily determined by high-accuracy photolithography.

From the above discussion it can be seen that the SAR ADC will take N steps (comparing and storing) for an N bit conversion to complete. In reality, the conversion time will also

depend on the DACs settling and converting speed. High resolution SAR ADC will take much longer time to finish converting than low resolution SAR ADC. For example 8 bit SAR ADCs can convert in a few hundred nanoseconds, while 16 bit ones will generally take several microseconds [20].

In summary, the SAR ADC architecture is widely used for low power applications. The resolution can be fairly high up to 10-12 bits [22,23,24]. The operating frequency usually is relatively low, in the Mega Hertz region.

1.2.3 Sigma-Delta ADC/Delta-Sigma ADC

Sigma-Delta modulation based analog to digital conversion technology is a cost effective alternative for high resolution (up to 24 bits [25]). It has been widely used for low cost, low bandwidth, low power and high resolution ADC. The sigma-delta concept was first filed for patent in 1954 and granted in 1960 [26]. The basic concept is the use of feedback for improving the effective resolution of a coarse quantizer. Figure 1.4 gives the block diagram of the first order modulator.

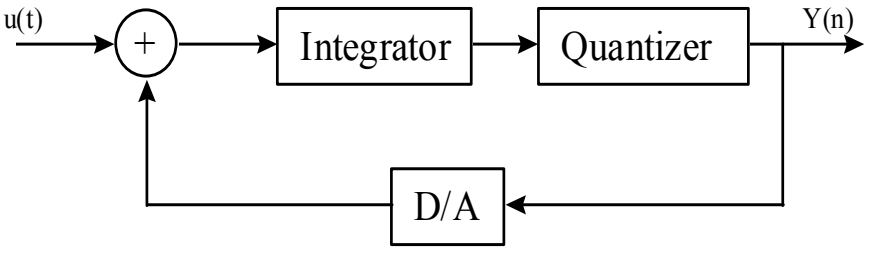

Figure 1.4 Block Diagram of First Order Modulator

As seen in Figure 1.4, the analog input u(t) gets to the quantizer via an integrator. The quantized output Y(n) is converted to an analog signal through the D/A converter, which

is fed back and subtracted from the input signal. This feedback forces the average value of the quantized signal to track the average of the input. Any persistent difference between them accumulates in the integrator and eventually corrects itself. In Z domain, the output Y(z) is the sum of a signal component U(z) and a quantization noise component E(z), i.e.,

$$\mathbf{Y(z) = S_{TF}U(z) + N_{TF}E(z)} \qquad \mathbf{(1.10)}$$

Where the signal transfer function is

$$S_{TF} = \frac{H(z)}{1 + H(z)}$$

And the noise transfer function is

$$N_{TF} = \frac{1}{1 + H(z)}.$$

If $H(z) = \frac{1}{z-1}$, then $S_{TF} = z^{-1}$ and $N_{TF} = (1-z^{-1})$ with $\left|N_{TF}\right| = 2\sin(\frac{\pi f}{f_s})$, where f_s is the sampling frequency. The signal is propagated with a delay, while the quantization noise is attenuated at low frequencies by the noise shaping of the discrete integrator.

Conventional high resolution ADCs, such as SAR ADC and flash type ADCs operate at the Nyquist rate (sampling frequency approximately equal to twice the maximum input signal frequency). These Nyquist samplers require an analog low pass filter (anti-aliasing filter) to prevent noise or unwanted signals outside the bandwidth from being aliased into the desired bandwidth. Sigma-Delta ADCs use a relatively low resolution ADC (usually the resolution is between 1 to 4 bit), noise shaping and very high over sampling ratio.

The resolution can be achieved by the filtering and decimation process. The theoretical maximum in-band signal to noise ratio of the output data stream of a first order modulator with an N bit quantizer is [27]

$$\mathbf{S/N(db) = 6.02N - 3.41 + 30log(OSR)} \qquad \mathbf{(1.11)}$$

The expression in (1.11) assumes the amplitude of the input sine wave is the maximum value (V_{Ref}) and the quantization noise has a spectral density that is uniform over the frequency range f_s. The oversampling ratio (OSR) is defined as OSR = $\frac{f_s}{2f_b}$ with f_b equals the bandwidth of the input signal.

The maximum in-band signal to noise ratio of the output data stream for a second order ΣΔ modulator with an N bit quantizer is

$$\mathbf{S/N(db) = 6.02N - 11.14 + 50log\ (OSR)} \qquad \mathbf{(1.12)}$$

Higher order ΣΔ modulators would result in a quantization noise transfer function

$$N_{TF} = (1 - z^{-1})^L \qquad \mathbf{(1.13)}$$

where L is the order of the modulator. The magnitude of the N_{TF} is given by

$$|N_{TF}(f)| = \left[2 \sin \frac{\pi f}{f_s}\right]^L$$

Thus the higher order modulator yields an increased attenuation of the quantization noise at low frequencies.

Equations (1.11) and (1.12) illustrate that large OSRs are required to obtain 12 to 16 bits resolution with single channel ΣΔ modulators. This is definitely a limiting factor for some high bandwidth applications. As will be discussed below, combining pipelining concept with Delta Sigma Modulation facilitates high resolution with relatively low OSRs.

Figure 1.5 shows the concepts of oversampling, digital filtering, noise shaping and decimation [28]. Figure 1.5A gives a perfect Nyquist rate sampling ADC which has quantization noise $q/\sqrt{12}$ distributed over a bandwidth of DC to fs/2 shown as the dot area. If a much higher sampling rate is chosen, like Kfs, the rms quantization noise will be distributed over the bandwidth of DC to Kfs/2. As shown in figure 1.5B, the noise in the bandwidth of DC to fs/2 is reduced and the unwanted noise can be filtered out by using a low pass filter, so the ENOB is improved. If we simply use oversampling to improve resolution, we must oversample by a factor of 2^{2N} to get an N bit increase in resolution. The sigma-delta ADC has a unique feature which shapes the low frequency noise to higher frequency that is out of the signal bandwidth as shown in figure 1.5C.

Based on its high resolution, combining with noise shaping and over sampling principle, sigma-delta modulation is a widely used technique for both A/D conversions and D/A conversions. The sigma-delta modulator combines both analog and digital circuit and introduces the challenges of a mixed signal integrated circuit.

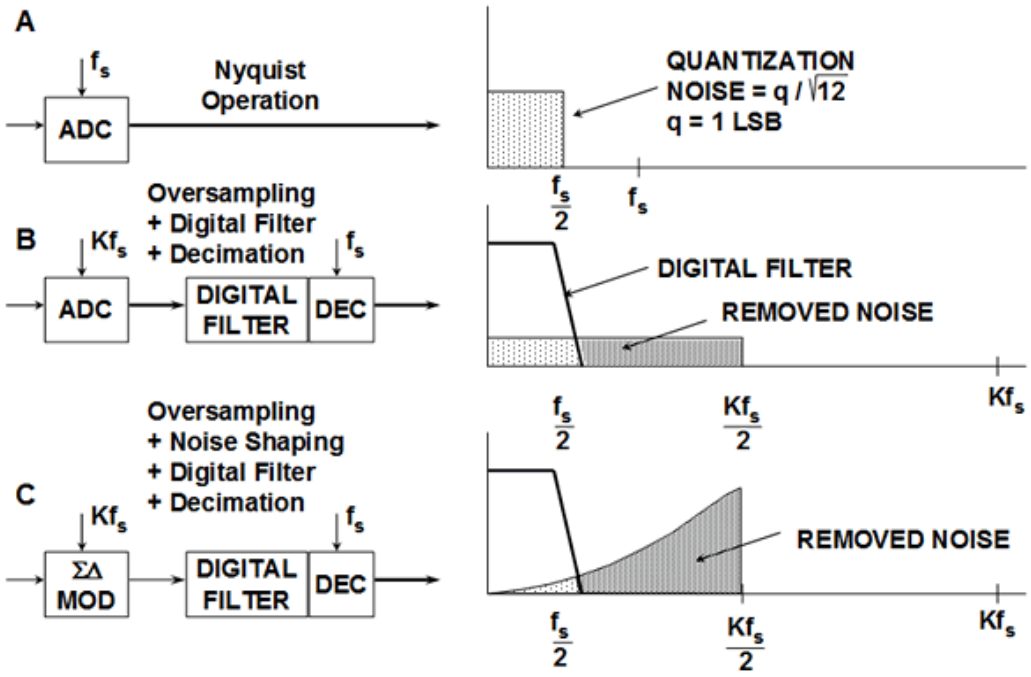

Figure 1.5 Delta Sigma Modulating Noise Shaping [28]

In general, sigma-delta modulator ADCs are widely used for low cost, high resolution, but low to medium bandwidth applications [29,30,31,32].

1.2.4 Pipelined ADC

The original pipelined ADC which was actually a multi-stage ADC was first used in the 1950s as a means to reduce the component count and power for flash ADCs [33,34]. The architecture is a typical sub-ranging ADC architecture as shown in Figure 1.6 [35] which has two stages of 3 bit ADCs. The analog input signal pass through a sample hold (SHA) circuit to keep the signal in hold mode during the conversion phase. The 1st stage flash ADC converts the SHA analog signal to 3 bit digital output which are stored in the output registers as the three most significant bits and also converted back to an analog signal using a 3 bit DAC. The amplified residual of the 1st stage goes to the 2nd stage flash

ADC and is converted to another 3 bit digital signal as the 3 least significant bits. This type of ADC is generally referred to as "subranging" because the input range is subdivided into a number of smaller ranges (sub-ranges) which are, in turn, further subdivided and the two stage conversion happening at the same SHA holding time. The focus for sub-ranging ADC is to minimize the number of components and power of the flash ADC, so to reduce the cost. This architecture requires $p*2^{n/p}$ comparators with n bit resolution comparing the 2^n -1 comparators of flash ADC, where p is the number of sub-ranging stages. However the conversion time which is the summation of p*one stage conversion time and (p-1)*(subtract + amplifier) delay time, is getting much longer than the flash ADC with only one stage of conversion. So this architecture could not be used for relatively high frequency applications until it is combined with a real pipelined concept.

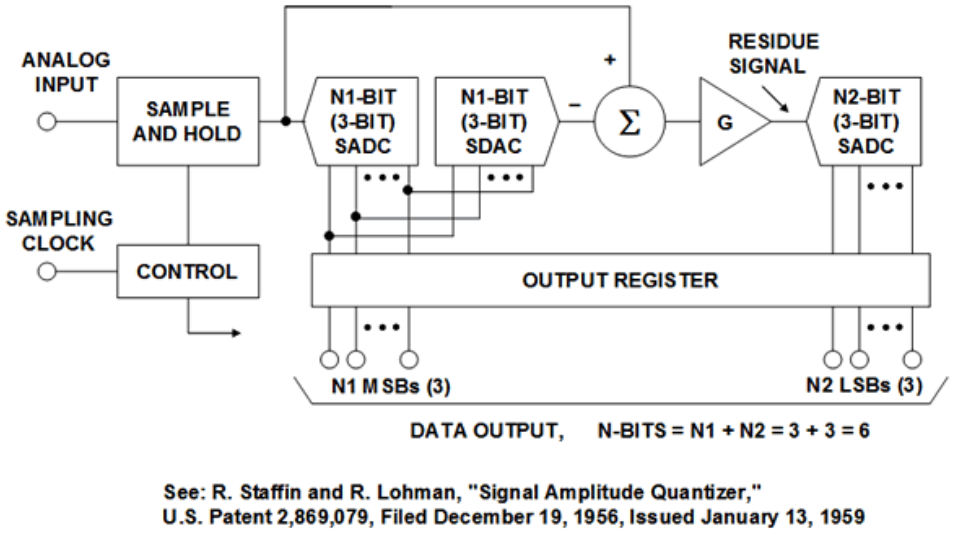

Figure 1.6 A 6-Bit, Two-Stage Sub-ranging ADC [36]

The Pipelined architecture is basically the same as sub-ranging with multi-stage operation, but each stage is separated by the registers as shown in Figure 1.7 [37]. For

the digital circuit, latches and D-flip flops are used for the register function; for the analog circuit, sample and hold circuits are used to implement the register function. Adding registers on each stage means each stage would have its own control clock. As long as the clocks for all stages are synchronized, the operating frequency only needs to meet each single stage time delay. Of course the outputs of all but the last stage in the "pipeline" must be stored in the appropriate number of shift registers, so that the digital data arriving at the correction logic corresponds to the same sample data. The Pipelined concept can be used in any circuit subsystem: analog, digital, ADC, DAC and so on.

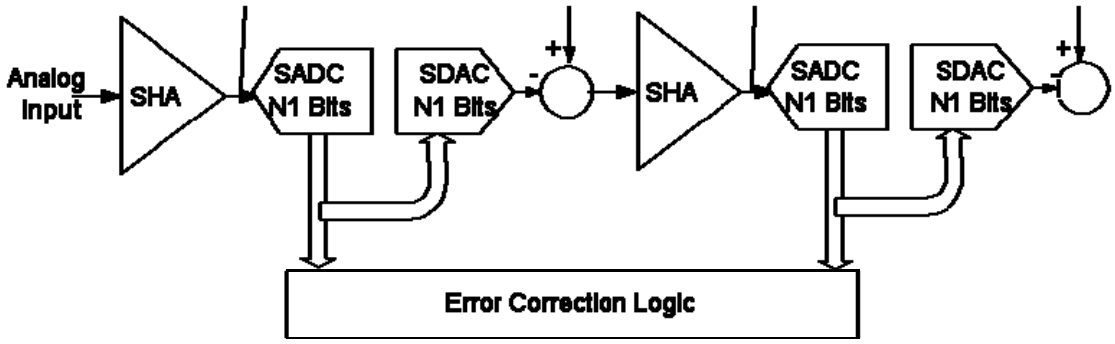

Figure 1.7 Generalized Pipelined Stages in a Sub-ranging ADC with Error Correction

Pipelined flash ADCs achieves broad band operation together with good resolution by using several consecutive stages of low resolution flash ADCs. This architecture requires $p*2^{n/p}$ comparators as part of the sub-ranging ADC advantage, so the accuracy of matching components is reduced and the flash architecture high speed feature is retained. However the high resolution pipelined ADCs require highly accurate and precise matching for each stage components such as DACs and analog buffers, delays, subtract circuits and amplifiers. Various ways of correcting the pipelined ADC errors have been

studied. An interleaved current pipelined ADC architecture based on a new high resolution Current Memory Cell was reported to reduce the signal-dependent charge-injection error [38]. A digital calibration technique which corrects errors due to capacitor mismatch and charge injection in pipelined ADC is given in [39,40]. Another way is background calibration in the analog domain using a pseudorandom dithering concept [41].

In general, the pipelined concept has been popular because combining pipelining with flash ADC architecture save power and components. Because of the limited resolution of flash ADC, it usually requires several stages of pipelined flash ADC to reach some decent high resolution. So the matching of each stage has become a problem. Achieving high bandwidth and high resolution ADCs in this way has been a challenge even with certain calibration techniques.

1.2.5 Time Interleaved ADC

For all the above discussion, the sampling frequency has to be at least twice the maximum input frequency of the ADC. This eliminates the use of CMOS technology for some broadband applications. One method of getting fast conversion is to use the slower ADCs in parallel with each sampling clock shifted, which is called time interleaving. The time interleaving concept is employed in ADC systems, which is then called time interleaved ADC. The basic architecture of the time interleaved ADC is shown in Figure 1.8 which has M channel N bit ADCs in parallel. For M channel time interleaved ADC, each channel only needs to operated at 1/M the overall system sampling rate (fs), but is clocked at a phase that enables the system as a whole to sample at equally spaced

increments of time which is time interleaved. The equally spaced increment of time is 1/fs. All channel digital outputs will be multiplexed out sequentially following the ADC time interleaving at fs frequency. For example, a four channel time interleaved ADC with a 2 GHz overall sampling rate is realized with each of the four channel ADC running at one-fourth of the system sampling rate, that is 500 MHz (2GHz/4), spaced at 0.5ns (1/2GHz) equal time intervals. The final digital data is streamed out by interleaving four of the individual channel data in the proper sequence with equal time spacing at 0.5 ns. This method eases the high speed requirement for each individual ADC components in which the overall system sampling rate can be really high. Unfortunately the resolution of these ADCs is low because of the mismatching between the ADC channels which include the gain, offset mismatching and time (jitter) error. Various correcting methods and study can be found in the literature [42,43,44,45].

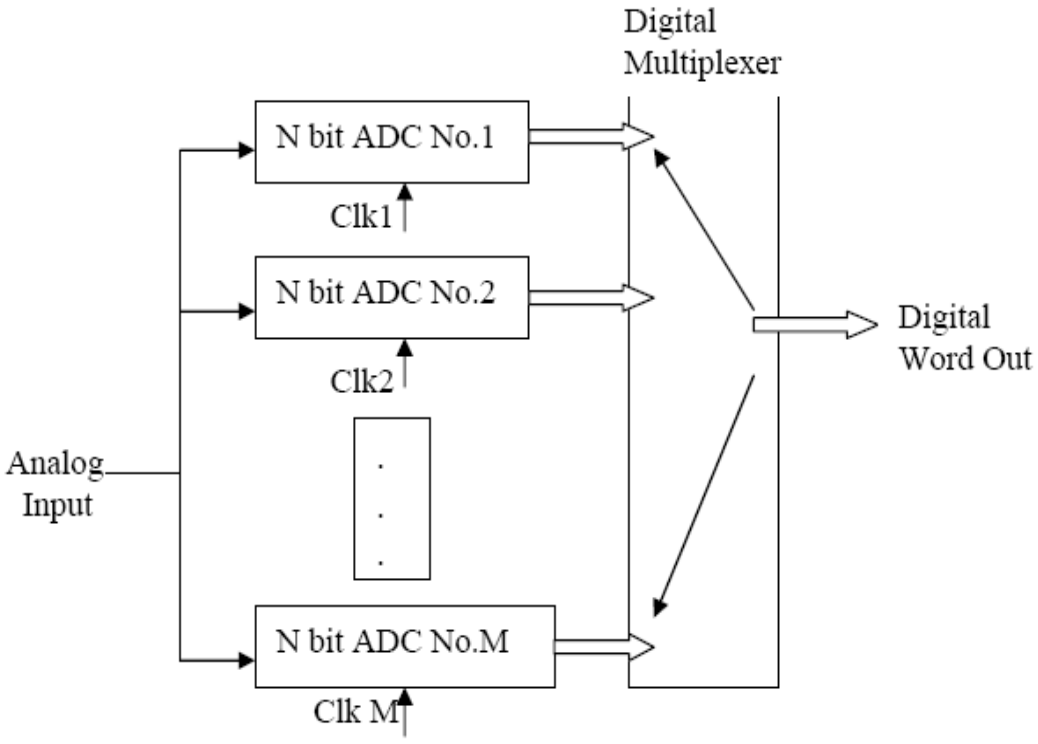

Figure 1.8 Time Interleaved ADC Architecture

1.3 Dissertation Motivation

The demand for low cost wireless communications during the last decade has dramatically increased, which in turn has driven the need for development of low cost system on chip transceivers. The broad objective is to develop components which support the design of a low cost receiver system. A typical RF receiver front end is shown in Figure 1.9. The received Radio Frequency (RF) signal from an antenna passes through a band pass filter (BPF1) and a Low Noise Amplifier (LNA) to retain some specified band pass RF signal. A direct conversion receiver convert the RF signal immediately following the LNA with no down convert mixer. Normally the RF signal frequency is too high for a standard ADC to process, so the 1^{st} stage down conversion mixer is used to reduce the RF to IF (Intermediate Frequency); usually the IF is still in the Gaga Hz range. If the ADC can operate at the IF range, then the 2^{nd} mixer can be eliminated. Otherwise it needs the 2^{nd} mixer to down convert the IF to BB (Base Band) frequency for low pass ADC to digitize the signal. The signal processing will follow the ADC to do some specified digital operations which is usually implemented by CMOS technology with low power and low cost features. So moving the digital signal closer to the front end receiver will be the main focus of this dissertation which includes the use of CMOS technologies to implement ADCs, on chip clocks and LO2 (Local Oscillator) subsystems as shown in Figure 1.9 with green color.

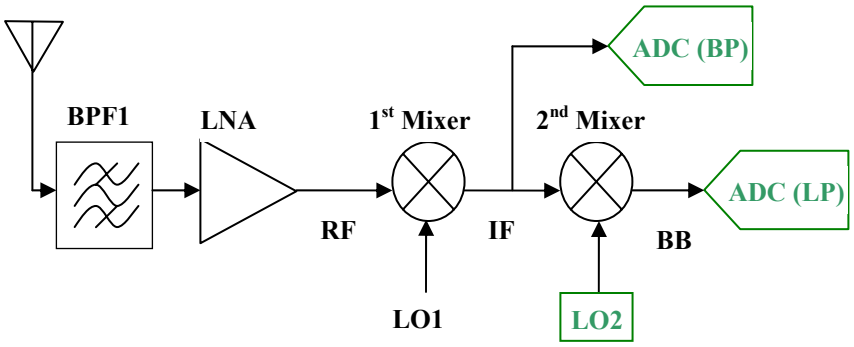

Figure 1.9 A Typical Direct Conversion Receiver Front End

It is well know that ADC is the bridge between the "real world" (analog signal) to the digital world which can operate at very high speed and low power with CMOS technology. The desire to move the analog to digital interface closer to the sensor has resulted in more stringent performance requirements for broad band, high resolution ADCs. To improve the ADC performance, some innovative technologies beside CMOS have been used, such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN) technologies with High Electron Mobility Transistors (HEMTs). Bipolar technology was mostly replaced by CMOS in digital applications because of increased component density and reduced power dissipation and cost. Now bipolar is becoming more popular again for mixed signal applications based on the speed. As far as is known, GaAs/GaN/HEMT technologies [46,47] are the fastest, but consumes highest power and are the most expensive technology. Also GaAs/GaN can not be implemented in the same substrate with CMOS circuits which is the cheapest, highest density and most popular used technology in the digital world. SiGe based BiCMOS technologies are not as fast as GaAs/GaN, but faster than pure CMOS. Currently there are many studies and even products which use BiCMOS technology. However, BiCMOS technology designs are more complex and use more power and have higher cost

compared to pure CMOS technology. So, this research will be focusing on the use of standard CMOS technologies to implement broad band ADCs, phase lock loops clock circuits and LOs to reduce power and cost.

A review of the most recent CMOS ADC papers has found that it's hard to get over 50 MHz bandwidth with moderate resolution (6-8bits) and even more difficult to achieve high resolution of 10 bits with CMOS technology. Many applications require wider bandwidth and higher resolution with relative low cost. The motivation of this dissertation is to investigate ADC architectures with high bandwidth and high resolution while using CMOS technologies for implementation.

1.4 Dissertation Objective

The first objective of this dissertation is to develop, implement and assess the performance of a unique CMOS low pass broad band, high resolution analog to digital converter architecture which is able to get 62.5 MHz bandwidth and up to 12 bit resolution. The second objective is to develop, implement, and assess the performance of a CMOS band pass ADC architecture that can be used for advanced receivers, where the feature of the ADC is to have flexible RF/IF center frequencies without changes in hardware. A third objective is to investigate, implement, and assess performance of CMOS on chip clock generation techniques that are essential to high sampling rate ADCs and mixer local oscillators.

2 Low Pass Pipelined Delta Sigma Modulator ADC

This chapter is going to present a unique Pipelined Delta Sigma Modulator (PDSM) ADC with an averaging (filtering) technique in both analog and digital domain [48,49]. High resolution, broad band operation is achieved by pipelining two or more stages of first order modulators with multi-bit quantization. First order modulators eliminate stability problems and also help to facilitate high sampling ratios. A unique analog averaging technique is used for generating the analog error input signal to the second (and subsequent) stages, which mitigates the effect of DAC nonlinearities and component accuracy of key analog circuits such as track/hold and subtract. This chapter will discuss the designing, fabricating, and testing of a PDSM ADC entire design cycle which including the following:

- Matlab/Simulink simulation to verify the viability
- Capture the entire system with TSMC0.18 process and simulate
- Customize layout the entire ADC including on chip clock generator and clock distribution trees
- Fabricate
- Design test fixture
- Test the prototype chip

2.1 Introduction

The analog to digital converter (ADC) has become a critical component for advanced telecommunication systems. The desire to move the analog to digital interface closer to the sensor has resulted in more stringent performance requirements for broad band, high resolution ADCs. The Flash ADC architecture is typically the fastest architecture. This architecture requires 2^n-1 comparators and 2^n equal resistors for providing the reference voltage to each comparator. The accuracy of the conversion is limited by component matching (comparators and resistors), so typically the flash architecture is only used for less than 8-bit resolution applications [13]. A popular ADC architecture for broad band applications is the Nyquist Rate Pipelined ADC [**Error! Bookmark not defined.**], [50,51]. The pipelined (or pipelined flash) ADC achieves broad band operation together with good resolution by using several consecutive stages of low resolution flash ADCs. This architecture requires $p*2^{n/p}$ comparators with p pipelined stages, so the requirement for accuracy of matching of some components is reduced and the flash architecture broadband feature is maintained. However the high resolution pipelined ADCs require highly accurate and precise matching for selected components such as DACs and analog buffers, delays, and subtract circuits. Delta Sigma Modulator ADCs reduce the requirements for highly accurate and matched components by incorporating over sampling and noise shaping [52,27,53,54,55]. This architecture has demonstrated resolutions as high as 20 bit with high over sampling ratio [56]. Broad band operation requires low over sampling ratios, which then limits the resolution. Several techniques have been used to increase the resolution of Delta Sigma Modulators with low over sampling ratios.

These techniques include increasing the order of the modulator to improve the noise shaping and using multi-bit quantization, or some combination of both [57, 58]. Another technique combines multiple higher order delta-sigma modulators in parallel [59]. Higher order modulators introduce stability issues; multi-bit quantization introduces DAC nonlinearity problems; and parallel delta-sigma architectures result in higher power and larger die area. Another approach uses cascading of multi-bit feed forward modulators to achieve higher order noise shaping [60], but this approach has problems with DAC nonlinearity, component accuracy and limited sampling rate. Averaging techniques have been used to reduce the offset specification for high speed A/D converters since 1990 [61]. This technique is limited to the flash architecture by taking the average value of neighboring node-voltages and thereby reducing the offset error. The modified averaging technique (interpolation averaging) has been employed to obviate the need for a large number of comparators or inter-stage digital-analog converters and residual amplifiers [62]. This technique is also used for the flash ADC. This chapter presents a unique Pipelined Delta Sigma Modulator (PDSM) ADC with an averaging (filtering) technique in both analog and digital domain [48]. High resolution, broad band operation is achieved by pipelining two or more stages of first order modulators with multi-bit quantization. First order modulators eliminate stability problems and also help to facilitate high sampling rates. A unique analog averaging technique is used for generating the analog error input signal to the second (and subsequent) stages, which mitigates the effect of DAC nonlinearities and component accuracy of key analog circuits such as track/hold and subtract.

2.2 Two Stage Pipelined Delta Sigma Modulator (PDSM) ADC Architecture

The architecture for the two stage PDSM ADC which incorporates a unique analog averaging technique is shown in Figure 2.1. As seen in Figure 2.1, the analog input signal is applied to a sample-hold circuit and then passes through a standard first order delta sigma modulator (green) with a discrete integrator, multi-bit quantizer. A four bit quantizer is used for this implementation and the clock frequency (fs) is 1.0 GHz. The 4-bit digital output signal of the quantizer passes through a two stage digital low pass filter (red) that reduces noise and increases the resolution of the digital signal to 7 bits. This 7-bit signal passes through another two stage digital low pass filter (red) which creates a 13-bit output. The 13 bit digital output is only accurate to 7-8 bits with an OSR of 8, but could be increased with a higher OSR (reduced input bandwidth or higher sampling rate). The second digital filter is needed in the first stage path to ensure the signals arriving at the Digital Error Correction Circuit from the first stage and the second stage have been subjected to identical filtering transfer functions.

Meanwhile, the original sampled signal has passed through a delay circuit which allows the sampled analog input and the sampled analog version of the 1st modulator output to be synchronized in time. The difference between the analog input signal and the analog version of the output of the first stage quantizer, which is called first stage analog error or residue is then amplified by 16 and passes through a two stage analog low pass filter (yellow) as seen in figure 2.1. The two stage analog filter has the same sampled data transfer function as the digital low pass filters of stage one to keep stage 1 and stage 2 matched precisely. The output of the analog low pass filter is then

amplified by 4 to obtain a total amplification factor of 64 before going to the 2nd stage first order delta sigma modulator. The second stage modulator (bottom blue blocks) functions are the same as the 1st stage. After passing through a two stage digital filter, the 2nd stage 4-bit quantizer output signal becomes a 10-bit digital word. The 10-bit signal created by the second stage is combined with the first stage 13 bits with the proper weighting by the digital error correction circuit to create a 16-bit output.

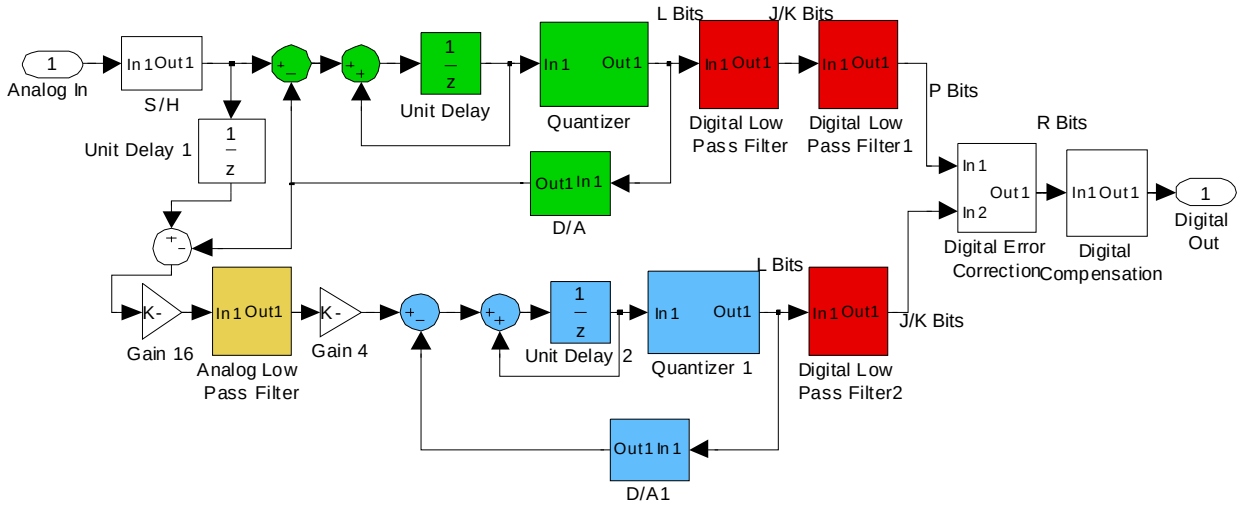

Figure 2.1 Two Stage PDSM ADC Architecture

A good candidate for both the digital and analog filters is a cascade of two low pass (SINC) averaging filters. The transfer function for each one of the averaging filters with length of M is

$$T_{ave}(z) = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i} \qquad \textbf{(2.1)}$$

The frequency response of Tave(z) can be expressed by equation (2.2):

$$T_{ave}(\omega) = \frac{\frac{1}{M}\sin(\frac{\pi M f}{fs})}{\sin(\frac{\pi f}{fs})} \approx \frac{\sin(\frac{\pi M f}{fs})}{\frac{M\pi f}{fs}} \equiv \sin c(\frac{\pi M f}{fs}) \qquad \textbf{(2.2)}$$

Each filter has its null at f=fs/M, so a reasonable choice for M is

$$M=OSR=fs/(2*Bandwidth) \quad \textbf{(2.3)}$$

For this application, the clock frequency (fs) is 1.0 GHz and input bandwidth is 62.5 MHz, which results in an over sampling ratio (OSR) of 8. So choosing M=OSR=8 results in the null at 125 MHz which is twice the input band width. The frequency response for the $[H_{SINC}(f)]^2$ filter is shown in Figure 2.2. The magnitude of the in band signals are attenuated by the $(SINC)^2$ function and must be precisely offset by a digital compensation filter after combining the first and second stage digital outputs [63].

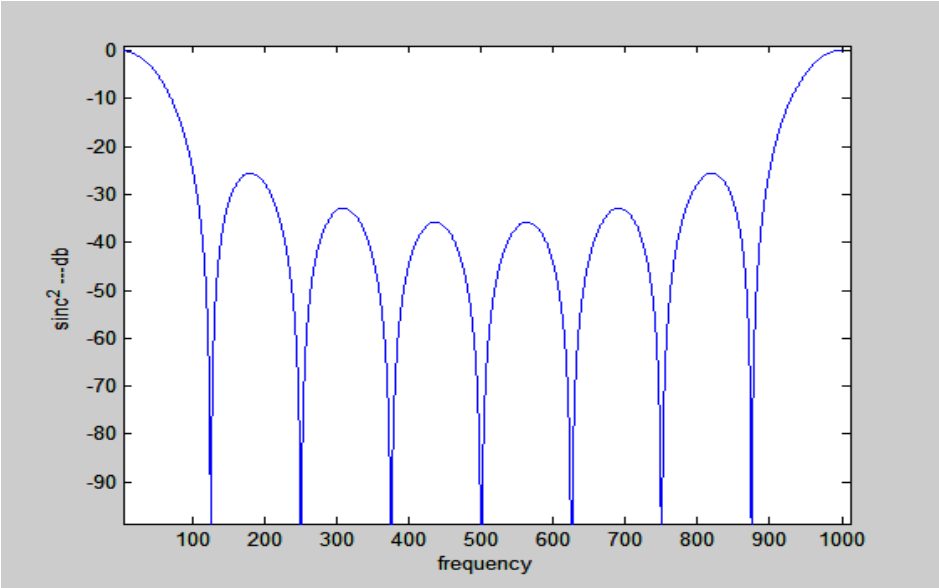

Figure 2.2 $T^2ave(\omega)$ Frequency Response with M=8, fs=1GHz

From the above discussion, it is seen that the difference between the analog input signal and the analog version of the output of the first stage quantizer (analog error or residue) is amplified by 16 and then passes through the analog low pass averaging filter. This results in the high frequency components of the error signal being attenuated, leaving a predominantly low frequency error signal (same bandwidth as the input signal) that after

amplifying has the same dynamic range as the analog input signal. In addition to reducing the bandwidth requirements for the analog amplifier multiplying circuits, the analog filter (averaging) of the error signal eliminates high frequency components of the noise on the error signal which reduces accuracy requirements for the sample hold circuits, the DAC, and the subtract/multiplier circuits. This is similar to the effect of oversampling on quantization noise. The noise generated by circuit inaccuracies on the 1 GHz sampled error signal will have some high frequency components outside the desired input bandwidth of 62.5 MHz. Filtering will reduce this noise power by eliminating the high frequency components. The filtered and amplified error signal is the input to the second stage first order modulator (blue) and the modulator outputs go to a digital low pass filter (low red) as seen in Figure 2.1. The digital output of the second stage digital filter (which is again a cascade of two SINC averaging filters) is the digital version of the error signal. The digital word is 10 bits wide, but only accurate to 5-6 bits. The digital outputs of the first stage and second stage are combined with the proper weighting to obtain an output that has 13-15 bit accuracy with MATLAB/SYMULINK simulations and 11-12 bit accuracy without the final compensation filter with transistor level Cadence designs. The oversampling with delta sigma modulation facilitates the use of relatively coarse 4 bit quantizers with associated component accuracy to ultimately generate 6-7 bit accuracy in each stage of the pipelined configuration. Note that both the first stage output and the second stage output is subjected to the same total filter transfer function of $(SINC)^4$.

2.2.1 Detailed Description of the PDSM ADC

A more detailed description of the PDSM ADC architecture is presented in the following.

2.2.1.1 Stage One

As stated earlier, the function of the first stage is to generate 10 most significant bits as well as generate the analog difference between the input signal and the analog equivalent of the 4 bit output of the first stage. Conventional pipelined ADCs use a flash ADC in each stage. The PDSM ADC incorporates first order delta sigma modulators and low pass averaging filters to produce more resolution in each stage. For general speaking, as seen in Figure 2.1 assume the delta sigma modulator of the first stage has an L bit output, which is the sum of signal component [z^{-1}Vin(z)] and a quantization noise component [$(1-z^{-1})$E(z)]. Vin(z) is the analog input to the modulator and E(z) is the quantization noise resulting from converting the input to an L bit digital signal. The signal component [z^{-1}Vin(z)] is the input signal delayed by one clock cycle, while the noise component [$(1-z^{-1})$E(z)] is shaped by the transfer function $(1-z^{-1})$. The magnitude of $(1-z-^{1})$ as a function of frequency is [48]

$$\left|1-z^{-1}\right| = 2\sin(\frac{\pi f}{f_s})$$

where fs is the sampling frequency of the modulator. Thus the quantization noise is diminished for input frequencies that are small compared to fs by the noise shaping transfer function. The amount of attenuation is proportional to the oversampling ratio which is defined as

$$\mathbf{OSR=fs/(2*Bandwidth)} \qquad \mathbf{(2.4)}$$

A well known maximum signal to noise ratio equation for a first order modulator with an L bit quantizer is [48]

$$\mathbf{S/N(db) =6.02*L - 3.41 + 30logOSR} \qquad \mathbf{(2.5)}$$

From Equation (2.5.), it is seen that if the output of the modulator is passed though a

perfect low pass filter to reject out of band noise, then the S/N ratio would be 50.7db for an OSR of 10 and L=4 bits. An S/N ratio of 50.7db corresponds to over 8 bits of resolution. Since the low pass filter is not perfect, the actual resolution is more likely to be 7 bits for an OSR of 10 and L=4 bits. In any case, it is seen that resolutions of 6 to 8 bits can be obtained in each stage of the PDSM ADC for L=4 and relatively low values of OSR.

The output of the digital low pass filter of the first stage (cascade of two SINC stages) will have J bits as seen in Figure 2.1, where J>L. For example, if L=4 bits and M=8 corresponding to an OSR=10, then J=10 bits. As discussed above, for an OSR=10, we can expect an accuracy of about K=7 bits at the output of the two stage low pass filter. The L bits of the quantizer output become the input to the D/A converter (L bit DAC). The output of the DAC is an analog signal which can be considered the sum of the analog input signal Vin(z), the quantization error E1(z) with noise shaped and the DAC error E_{DAC}; ie,

$$\mathbf{Vd(z)=Vin(z)+ E1(z) + E_{DAC}(z)} \qquad \mathbf{(2.6)}$$

The output of the DAC Vd(z) is an input to the analog subtract circuit. Another input to the analog subtract circuit is the analog input signal Vin(z) after passing through a delay block. The output of the subtract is the 1st stage noise shaped quantization error which has to be amplified to reach the normal dynamic range. The amplified analog error signal which is $(Vin(z)-Vd(z))*2^L = [E_A(z)-E1(z)]*2^L$, goes through a cascade of two analog SINC averaging filters (low pass filter), where $E_A(z)$ includes the DAC, S/H and subtract errors. The low pass filter rejects much of the quantization noise that has been shifted to higher frequencies by the delta sigma modulator noise shaping, so Vd(z) is now a signal that has been limited to frequencies that are approximately equal to the bandwidth of the

input. The analog averaging filters can be realized in a straight forward manner with a circular buffer track and hold circuit and analog adder. The frequency response of the analog low pass filter is exactly the same as the digital low pass filter, so the output of the analog low pass filter is

$$V'in(z)= 2^{L} [E_A(z) -E1(z)]Tave(z)]^2 \qquad (2.7)$$

It is very important that the analog and digital low pass filter have identical transfer functions and that is the reason for choosing the SINC averaging filters.

For traditional pipelined ADCs, the output of the DAC is an unfiltered sum of the input signal and the quantization noise of flash first stage ADC. The quantization error from a flash ADC has a uniform spectral density function (constant over frequency from 0 to $f_s/2$). Thus the quantization error has a magnitude that uniformly distributed between +/- $\Delta/2$ (where Δ is the resolution of the flash ADC) and has a frequency that is equally likely to be any value from 0 to $f_s/2$. On the other hand, for the PDSM ADC, the quantization noise at the output of the delta sigma modulator has been shifted to higher frequencies by the modulator noise shaping and the low pass filter rejects most of the high frequency noise components to reduce the power of the quantization noise and increase resolution of the first stage from L to J bits. It is also noted that any non-linearity error of the first stage quantizer would be included in the error denoted as $E_1(z)$ above and offset by the error correction. The final operation of the first stage is to multiply the output of the subtract circuit by 2^{J-L-1} to obtain a signal that has the same dynamic range as the input. So the output of the second analog multiplier of the 1st stage as shown in Figure 2.1 is

$$V''in(z)= [E_A(z)-E_1(z)]2^{J-1} T^2ave(z) \qquad (2.8)$$

2.2.1.2 Stage Two

The output of the second analog multiplier of the first stage is the input to the second stage modulator. The second stage modulator/low pass filter combination operate in the same manner as the first stage to produce a J bit digital representation of the amplified analog quantization error, $[E_1(z)\ 2^{J-1}\ T^2ave(z)]$. The J bit output of the low pass filter can be expressed as

$$\mathbf{V_{dJ}(z)=\{[E^A(z)-E_1(z)]2^{J-1}\ T^2ave(z)+E_2(z)\}\ T^2ave(z)} \qquad \mathbf{(2.9)}$$

where $E_2(z)$ is the noise shaped quantization error of the second stage modulator.

Again referencing to Figure 2.1, the first Sinc filter of the first stage PDSM generates K bit outputs, but would only accurate to J bit. The J bit digital output of the first stage is passed through a second digital low pass averaging filter to produce a P bit signal that can be expressed as

$$\mathbf{V_{dP}(z)=[Vin(z)+\ E_1(z)]\ T^4ave(z)} \qquad \mathbf{(2.10)}$$

The digital error correction circuit adds $V_{dJ}(z)$ and $V_{dP}(z)$ after shifting $V_{dJ}(z)$ J-1 places to the right (divide by 2^{J-1}) to obtain a R bit signal

$$\mathbf{V_{dR}(z)=[Vin(z)+E_A(z)]T^4ave(z)+\ E_2(z)T^2ave(z)/\ 2^{J-1}} \qquad \mathbf{(2.11)}$$

As discussed above, the low pass filters of the second stage increase the bits that are combined in the digital error correction circuit causing more overlap and some randomizing of the interface between the two signals.

Finally the R bit signal $V_{dR}(z)$ is passed through a digital reconstruction filter (and a decimation circuit if needed). The digital reconstruction filter has a frequency response of $T^{-4}ave(z)$ for frequencies in the pass band, so it compensates for the amplitude reduction caused by the averaging filters. The digital reconstruction filter would be

designed to reject signals with frequencies higher than the pass band, including quantization noise. This facilitates obtaining a final resolution of N bits where N>2J.

2.2.2 Summary

Thus the PDSM ADC allows high resolution with only two stages and with relatively low over sampling ratios and relatively high bandwidths. In addition, the accuracy requirements of key components in the first stage (digital to analog converter, analog subtract, and analog multiply) are reduced because of the action of the analog and digital low pass filters of the second stage. The cascade of two averaging filters of length M causes a randomizing of component mismatch errors and other uncorrelated errors which will tend to average to zero. The digital low pass filters of the second stage also increase the number of bits that are combined in the digital error correction circuit resulting in some randomizing of the interface between the two signal being combined. This helps to reduce component accuracy requirements and eliminated the need for sophisticated error correction techniques. Similarly, the analog low pass filter of the first stage helps to reduce the accuracy requirements of the first stage analog track and hold and adder circuits. Also the errors due to non-linearity of the first stage L bit quantizer will be included in the first stage error signal and will be canceled out by the digital correction circuit at the output of the PDSM ADC.

The PDSM ADC provides the potential to increase the bandwidth/resolution envelope compared to currently available ADCs.

Some key features of the PDSM ADC architecture are:

- High resolution and broad band operation with relatively low OSR

- Accuracy requirements for track and hold circuits, analog subtract circuits, and DAC are mitigated by the analog averaging of the error signal
- Over all component matching and accuracy requirements are reduced by the over sampling delta sigma configuration
- Nonlinearity of the first stage DAC/quantizer is included in the error signal and the effect of the nonlinearity is reduced when the second stage output is combined with first stage output
- Pipeline operation is based on first stage generating 6-7 most significant bits and second stage generating 5-6 least significant bits using first order delta sigma modulators.
- PDSM architecture differs from MASH or feed forward architectures that seek to obtain higher order delta sigma operation. First order modulators used by PDSM ADC facilitate high sampling rates.

2.3 Matlab Simulink Model Design

The PDSM ADC two stage architecture as shown in Figure 2.3 was captured using the MATLAB/SIMULINK simulator to verify the feasibility of obtaining the high resolution/broad bandwidth performance. The delta sigma modulators are implemented with an adder/integrator and a 4 bit quantizer as shown in Figure 2.4. All the analog mathematical functions are implemented ideally. The cascaded averaging filters are of length M=8 and are realized by using the appropriate SINC transfer function in the z domain as shown in Figure 2.5, $T(z) = \frac{Z^8 - 1}{Z^8 - Z^7}$. The sampling frequency is 1 GHz

and the analog input signal is in the frequency band of 0 to 62.5 MHz. The Fast Fourier Transform (FFT) of the output signals are shown in Figure 2.6 for an input of 50 MHz, Figure 2.7 for an input of 10 MHz, Figure 2.8 for an input of 25MHz.

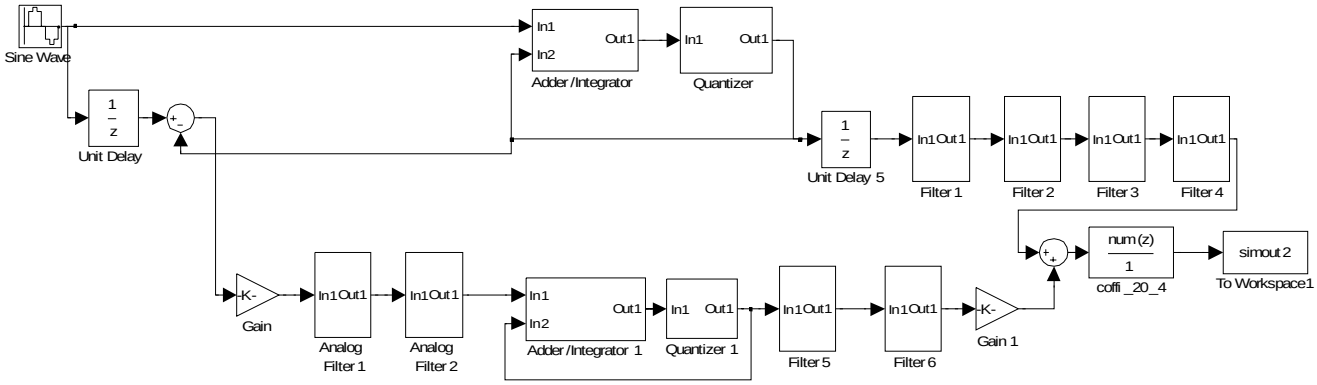

Figure 2.3 Two Stage PDSM ADC Simulink Model Block

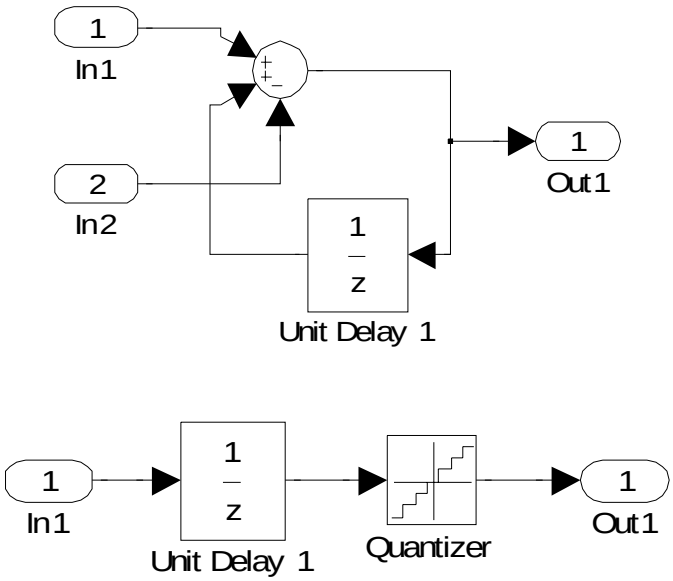

Figure 2.4 Delta-Sigma Modulator and Quantizer Simulink Models

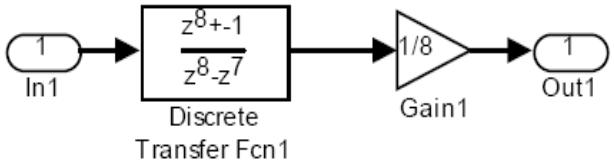

Figure 2.5 One Stage Averaging Filter Simulink Model

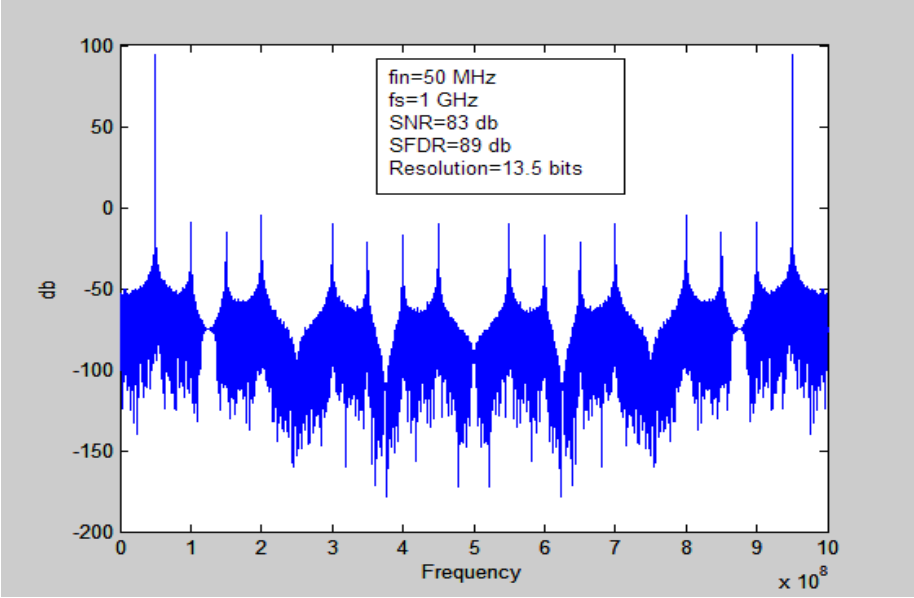

Figure 2.6 Matlab FFT Results for 50 MHz Input

The above FFT results indicate that the two stage PDSM ADC has a resolution of 13.5 effective bits for a 50 MHz input. The Spur Free Dynamic Range (SFDR)=89 db for 50 MHz input. The FFT of the output signal for a 10 MHz input and a 25 MHz are shown in Figure 2.7 and 2.8 respectively. The resolution is 15 effective bits and the SFDR is 106 db for both 10 MHz and 25 MHz inputs.

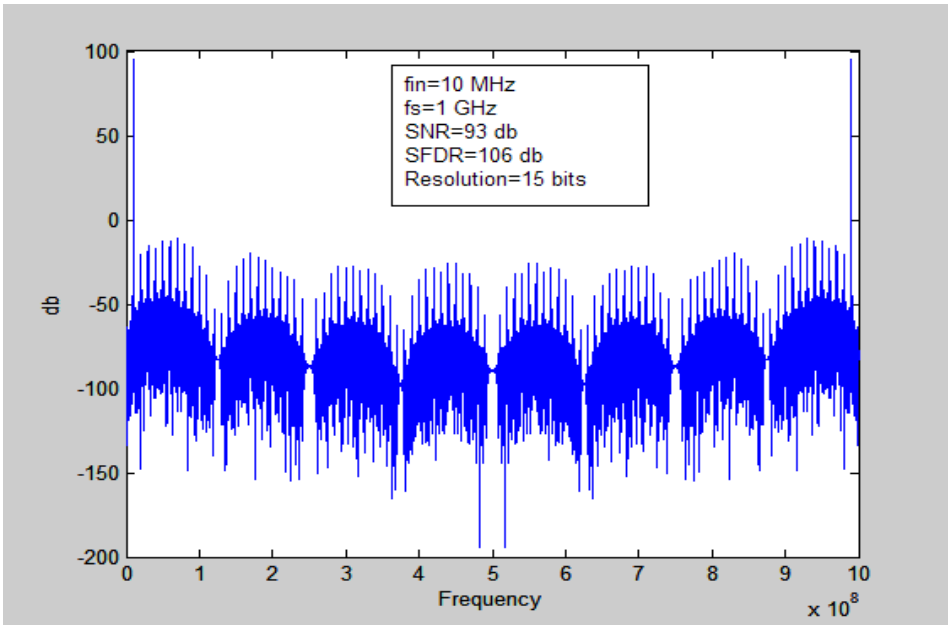

Figure 2.7 Matlab FFT Results for 10 MHz Input

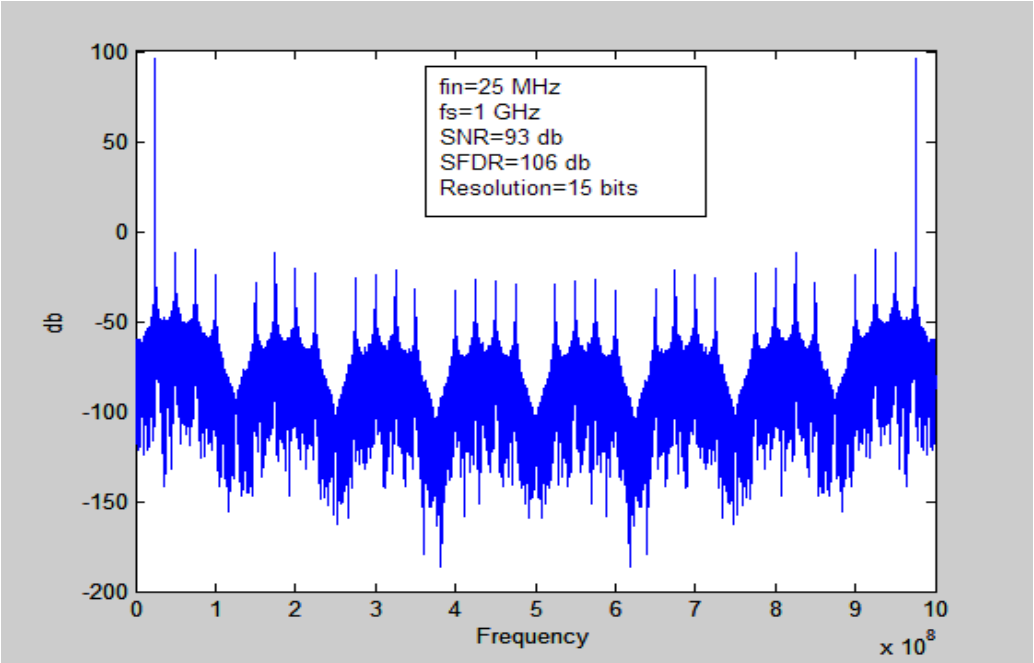

Figure 2.8 Matlab FFT Results for 25 MHz Input

2.3.1 FIR Compensation Filter Design for Two Cascaded Low Pass SINC filters

As discussed before, Δ-Σ Modulator ADC shapes the magnitude of the quantization noise so that the noise is reduced at lower frequencies and increased at higher frequencies. If the input signal is confined to a relatively small band compared to the ADC sampling frequency, then the resolution is increased by passing the digital output of the Δ-Σ Modulator through a low pass filter. A hardware implementation of a Δ-Σ Modulator ADC must include a low pass filter at the output of the Δ-Σ Modulator. For example, a first order Δ-Σ Modulator would incorporate a cascade of two digital SINC low pass filters to reject the high frequency quantization noise [64,65]. The transfer function for a cascade of two SINC filters which is used in this PDSM ADC architecture is

$$[H_{SINC}(f)]^2 = \left(\frac{\sin(M*\pi*F)}{M*\sin(\pi*F)} \right)^2 \qquad \textbf{(2.12)}$$

Where F=f/fs. The first notch of the SINC filter occurs at f=fs/M as shown in Figure 2.2, so the input signal bandwidth fb is usually limited to frequencies fb< fs/(2M). Ideally the low pass filter should have a magnitude of one in the frequency range of 0 to fb; however the SINC filter has a droop in magnitude that must be precisely compensated by a digital compensation filter. Thus in the pass band, the compensation filter must have a transfer function $H_{FIR}(f)$ so that $H_{FIR}(f)*[H_{SINC}(f)]^2$ has a value of one with an error that is less than the resolution of the ADC. If the resolution of the ADC is 8 bits, then the error must be less than 2^{-8}. At the same time, the gain of the compensation filter in the stop band must be such that $H_{COMP}(f)*[H_{SINC}(f)]^2$ is small enough so that the noise is sufficiently rejected outside the pass band to support the 8 bit resolution. A block diagram of the Δ-Σ Modulator (DSM) ADC with two low pass cascaded SINC filters and compensation filter is shown in Figure 2.9.

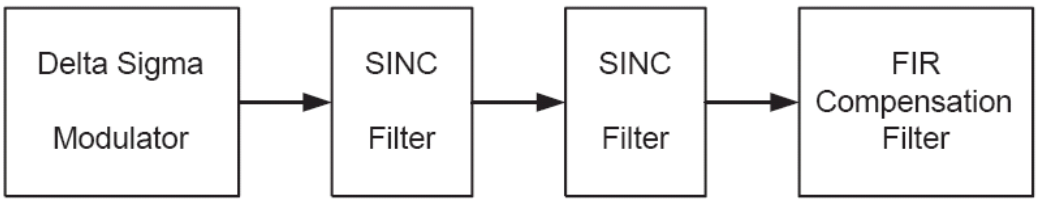

Figure 2.9 DSM Block Diagram with Compensation Filter

The transfer function for an FIR filter has the form

$$H_{FIR}(Z) = \frac{a_0 Z^{-0} + a_1 Z^{-1} + \ldots + a_n Z^{-n}}{1} \qquad \textbf{(2.13)}$$

For a linear phase FIR filter, the coefficients are symmetrical so that $a_0=a_n$, $a_1=a_{n-1}$, ... The frequency response of a linear phase FIR filter of order 2L+1 is given by

$$H_{FIR}(f) = h(0) + 2\sum_{k=1}^{L} h(k)\cos(2k\pi F) \tag{2.14}$$

where F=f/fs and h(k) are the filter coefficients

Equation (2.14) can be written in vector form as

$$H_{FIR}(f) = d^{T}.h \tag{2.15}$$

where d^T = [1 2cos(2πF) 2cos(4πF) … 2cos(2LπF)] and

$$\mathbf{h^T = [h(0)\ h(1)\ \ldots\ h(L)]} \tag{2.16}$$

The coefficient vector h will be uniquely determined if we specify a desired response for L+1 frequencies. That is

$$H_{IFIR} = \begin{bmatrix} H_{IFIR}(0) \\ H_{IFIR}(f_1) \\ \vdots \\ H_{IFIR}(f_L) \end{bmatrix} = A.h \tag{2.17}$$

Where A is a L+1 by L+1 matrix as shown below

$$A = \begin{bmatrix} 1\ 2 & \ldots & 2 \\ 1\ 2\cos(2\pi\frac{f1}{fs}) & \ldots & 2\cos(2L\pi\frac{f1}{fs}) \\ \vdots & & \\ 1\ 2\cos(2\pi\frac{f_L}{fs}) & \ldots & 2\cos(2L\pi\frac{f_L}{fs}) \end{bmatrix}_{(L+1)*(L+1)} \tag{2.18}$$

If H_{IFIR} is specified, then h is uniquely found from $h=A^{-1}*H_{IFIR}$. We require that $H_{FIR}(f)*[H_{SINC}(f)]^2=1$ with an error that is less than 2^{-8} for a resolution of 8 bits for $0 < f <$ fb, where fb is the bandwidth of FIR filter. Thus we choose,

$H_{IFIR}(0) = 0$, $H_{IFIR}(1) = 1/[H_{SINC}(f_1)]^2$,

$H_{IFIR}(2) = 1/[H_{SINC}(f_2)]^2$, …

$H_{IFIR}(m) = 1/[H_{SINC}(f_m)]^2$

for $f_m <= f_b$

The number of points $f_0, f_1, \ldots, f_m$ must be sufficient to get the required accuracy for the compensation filter response for all frequencies between 0 and fb. If our bandwidth is 62.5 MHz, then we must specify enough points in the 0 to 62.5 MHz range to get

$$H_{IFIR}(i) = \frac{1}{\left(H_{SINC}(fi)\right)^2}.$$

For $f_b < f_m < f_{st}$ is the transition region, where f_{st} is the stop band frequency. Transition region is defined as the region where the compensation filter transit from a value of $H_{FIR}(f)= 1/[H_{SINC}(fb)]^2$ to a value of 0. The transition region is determined by specifying values for $H_{IFIR}(i)$ in the region $f_b < f <$ fst.

For frequencies higher than f_{st} is the stop band region; we specify a number of points where $H_{IFIR}(i)=0$ as the stop band value.

2.3.1.1 FIR Compensation Filter Design Example

To illustrate the design technique, we consider a first order Δ-Σ Modulator ADC with a sampling frequency of 1.0 GHz and a band width of 50 MHz. A MATLAB program has been written to implement the previously described technique. The input to the program is the frequency vector $f=[f_0,f_1,\ldots f_L]^T$ which specifies the frequencies for calculating the vector

$$H_{IFIR} = \begin{bmatrix} H_{IFIR}(0) \\ H_{IFIR}(f_1) \\ \vdots \\ H_{IFIR}(f_L) \end{bmatrix} \qquad \textbf{(2.19)}$$

Then the filter coefficients h(i) are calculated using $h = A^{-1}*H_{IFIR}$ as discussed above. In this example, the frequency vector f is selected with values from 0 to 500 MHz. We have an objective of meeting the performance requirements (8 bits resolution) using a Linear Phase FIR compensation filter with a total of 41-tap. The vector f should have 21 points in this case. Specifically $f=[0\ 14\ 28\ 38\ 45.5\ 49.5\ 100\ 140\ 170\ 200\ 225\ 250\ 275\ 300\ 325\ 350\ 375\ 400\ 430\ 460\ 490]^T$. The first six values (MHz) are in the pass band, so H_{IFIR} (f) is set equal to $1/[H_{SINC}(f1)]^2$ at these six frequencies. The value of 100 MHz is in the transition region and H_{IFIR} (f) is given a value of 0.1 at this frequency. For the last 14 frequencies, H_{IFIR} (f) are assigned values of 0.0 as stop band region. Then the filter coefficients are determined by solving the linear matrix equation $h = A^{-1}*H_{IFIR}$. This yields 21 values for the filter coefficients, and the other 20 are the symmetrical counterparts, so the 41 filter coefficients are uniquely determined. The specific values resulting from this example are

h= [-0.70 2.09 -1.76 0.74 -1.26 0.40 0.34 0.26 0.74 -0.53 0.24 -0.74 0.04 -0.39 0.05 -0.02 0.28 0.14 0.41 -0.02 0.36 -0.02 0.41 0.14 0.28 -0.02 0.05 -0.38 0.04 -0.74 0.24 -0.53 0.74 0.26 0.34 0.40 -1.26 0.74 -1.76 2.09 -0.70]^{T}.

Note that the coefficients are rounded at the second decimal point to limit the digital word width of the coefficients to 8 bits. The resulting frequency response for the FIR compensation filter is shown in Figure 2.10.

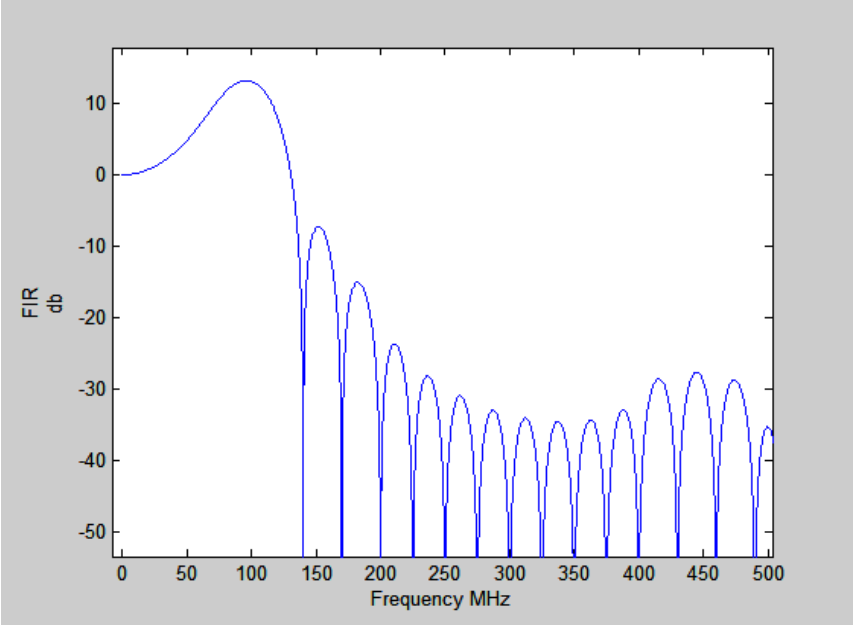

Figure 2.10 Frequency Response for 41-tap FIR Compensation Filter

As seen in Figure 2.10, the frequency response of the FIR compensation filter is equal to $1/[H_{SINC}(f1)]^2$ in the pass band of 0 to 50 MHz. The combined frequency response for the cascaded SINC low pass filter and the 41-tap FIR compensation filter is shown in Figure 2.11.

From Figure 2.11, it is seen that the combined frequency response has a value of 0 db in the pass band. The transition to the stop band is relatively sharp and the stop band is sufficiently low to yield a signal to noise ratio for the required resolution.

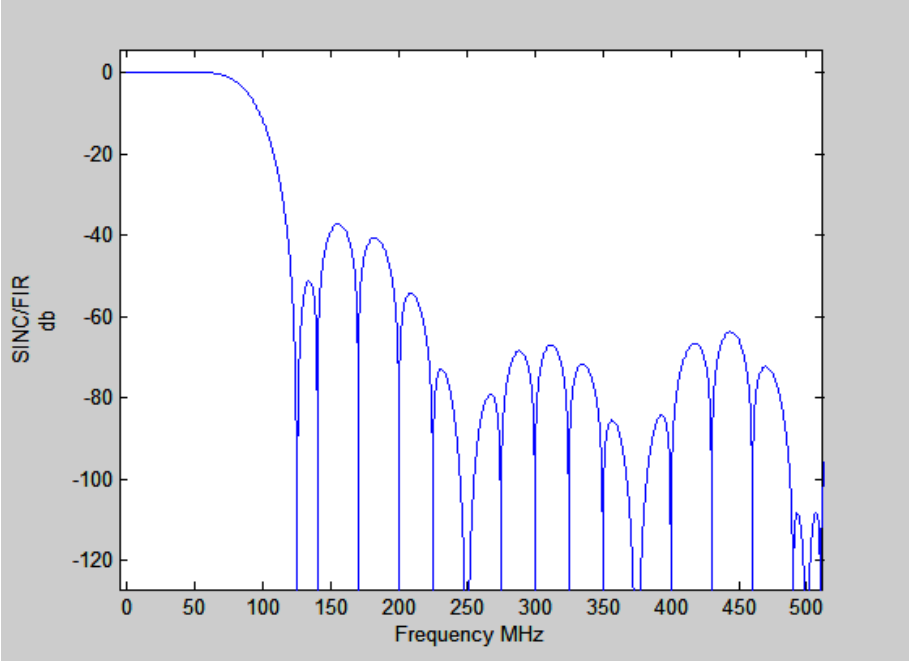

Figure 2.11 Combined Frequency Responses of Cascaded SINC Filters and 41-tap FIR Compensation Filter

2.3.1.2 FIR Digital Filter Implementation Technique [66]

The filter coefficients for the 41-tap linear phase FIR compensation filter is converted to binary value and shown in Table 2.1.

Finite Impulse Response (FIR) filters are digital filters that have a unit impulse response that is finite duration. Figure 2.12 Direct Form FIR Filter Design illustrates the direct form FIR filter. The implementation of the filter requires L multiplications and L additions for each output sample. The transfer function for the direct FIR filter can be expressed as:

$$H(z) = \sum_{k=0}^{L-1} h(k) z^{-k} \qquad \textbf{(2.20)}$$

where L is the number of taps.

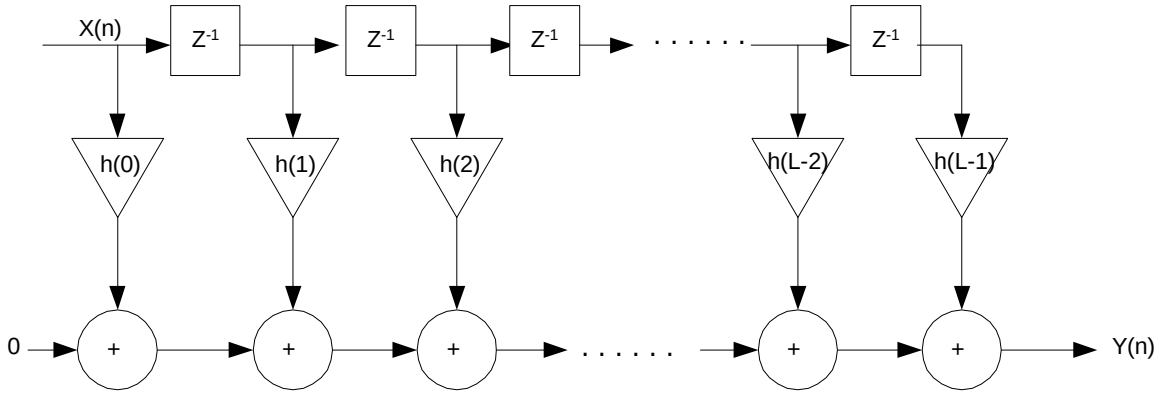

Figure 2.12 Direct Form FIR Filter Design

Linear phase FIR filters are used in this design because the phase shift of the output is a linear function of the frequency and it has a symmetrical property. The symmetrical property of linear phase FIR filter allows us to design a hardware reducing configuration filter where the delayed signal is fed back to halve the number of multipliers required [67] as shown in Figure 2.13. Since two of the samples will be multiplied by the same coefficient, instead of multiplying them separately, they can be first added together, and then multiplied by their common coefficient. Although extra summing adders are required, it has only half the number of inputs and thus is simpler to implement [67]. The linear phase FIR filter implementation saves about one half of the multiplications required from L to $(L/2) + 1$, therefore it requires far less computational effort compared to the direct form FIR filter. The transfer function for the linear phase FIR filter can be expressed as:

$$H(z) = z^{-L/2}[h(0) + \sum_{k=1}^{L/2} h(k)(z^{k} + z^{-k})] \qquad \textbf{(2.21)}$$

Table 2.1 Filter Coefficients for 41-Tap Linear Phase FIR Filter

Taps	Coeff.	Coeff. in Binary
20	0.36	000.010111
19, 21	-0.02	100.000001
18, 22	0.41	000.011010
17, 23	0.14	000.001000
16, 24	0.28	000.010001
15, 25	-0.02	100.000001
14, 26	0.05	000.000011
13, 27	-0.39	100.011000
12, 28	-0.04	100. 000010
11, 29	-0.74	100.101111
10, 30	0.24	000.001111
9, 31	-0.53	100.100001
8, 32	0.74	000.101111
7, 33	0.26	000.010000
6, 34	0.34	000.010101
5, 35	0.40	000.011001
4, 36	-1.26	101.010000
3, 37	0.74	000.101111
2, 38	-1.76	101.110000
1, 39	2.09	010.000101
0, 40	-0.70	100. 101100

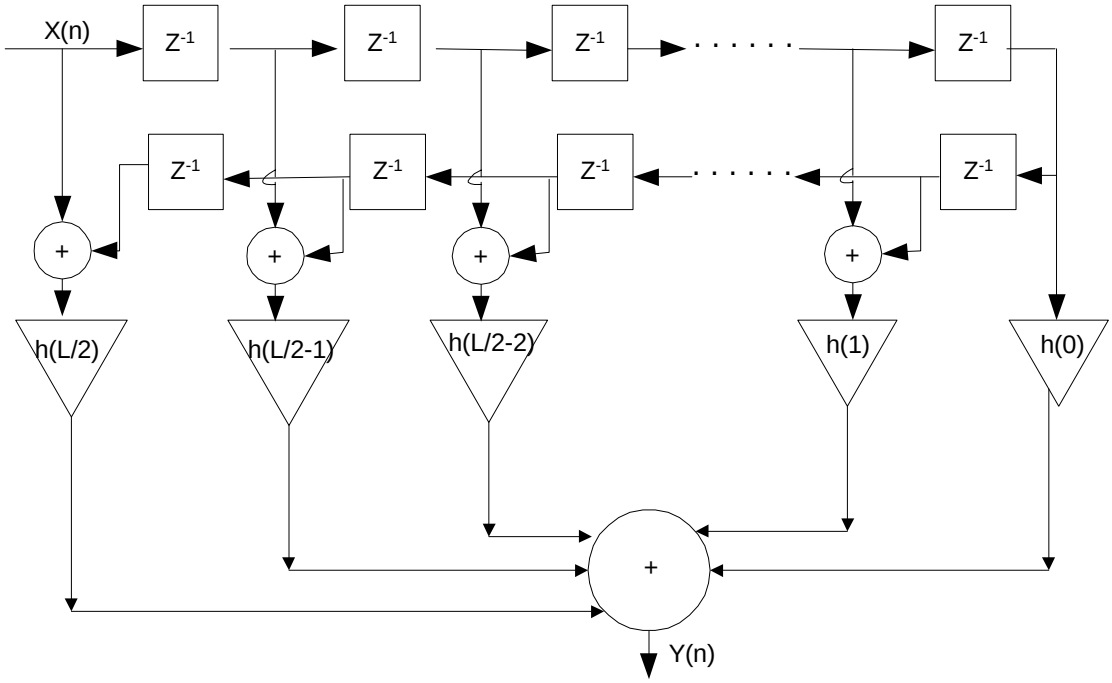

Figure 2.13 Linear Phase FIR Filter Design

The following will demonstrate the MatLab/Simulink simulation results. The detail compensation FIR filter hardware design can be found in reference [66] as a separate project off this dissertation.

2.3.2 MatLab/Simulink Simulation Results with FIR Compensation Filter

This is verified by running a MATLAB/SIMULINK simulation of the one stage PDSM ADC as shown in Figure 2.14 with the FIR compensation filter as described above.

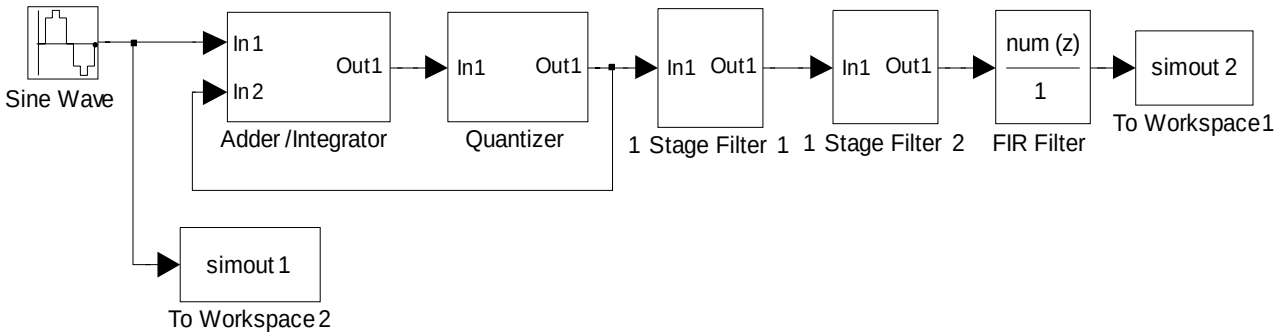

Figure 2.14 One Stage PDSM ADC Simulink Simulation Model

An FFT is performed on the output and the signal to noise ratio is calculated over the entire band width of 0 to 500MHz (fs/2). The FFT results are shown in Figure 2.15 below.

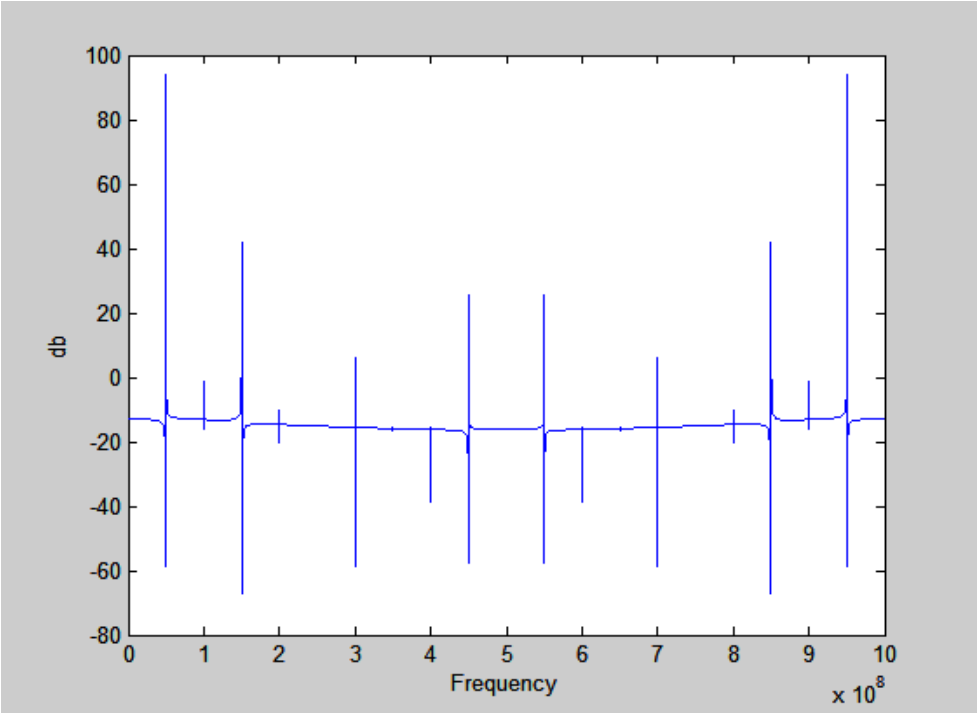

Figure 2.15 FFT Results DSM ADC 50 MHz Input with FIR Compensation Filter

The results shown in Figure 2.15 are based on a two stage cascaded SINC filter with M=8 and the 41 tap linear phase FIR compensation filter with 8 bit coefficients as described above. The clock frequency is 1 GHz. From the results, the signal to noise ratio is

calculated over the entire frequency range of 0 to 500 MHz and is found to be 51 db. This corresponds to a resolution of 8.2 bits, which satisfies the design objective. In conclusion, the FIR compensation filter offsets the droop of the cascaded SINC low pass filters with the required accuracy of 8 bits in the pass band. The combined frequency response of the cascaded SINC filters and the FIR compensation filter sufficiently rejects the quantization noise in the stop band to yield a signal to noise ratio that is consistent with 8 bit resolution. The design example illustrated a 41 tap linear phase FIR filter with 8 bit coefficients that satisfied the design objective of 8 bits resolution for 50 MHz band width and 1 GHz sampling frequency. The SINC filter implementation requires no multiplies and the 41 tap linear phase FIR filter requires 21 8X8 multiplies. If a single FIR filter is used for the low pass filter (No SINC Filters), 55 taps would be required for a linear phase implementation requiring 28 8x8 multiplies. It is estimated that the implementation using the SINC filters and the hardware efficient FIR compensation filter saves about 21 % in hard ware (chip area). Also the use of the digital Sinc filter permits implementation of a matching analog sampled data version of the Sinc filter which is needed for the PDSM ADC realization.

To analyze the FIR compensation filter effect to the discussed Delta Sigma Modulator ADC, a MatLab Simulink Model is built as shown in Figure 2.16 which does not have the FIR compensation filter.

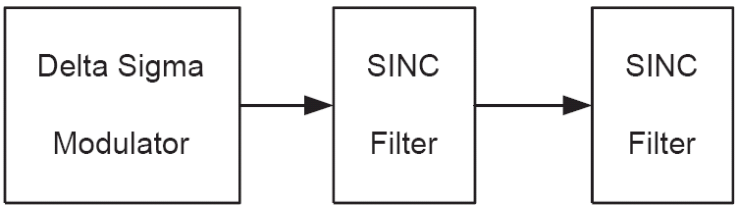

Figure 2.16 DSM Block Diagram without Compensation Filter

The Simulink simulation model is shown in Figure 2.17. The output FFT simulation result is given in Figure 2.18.

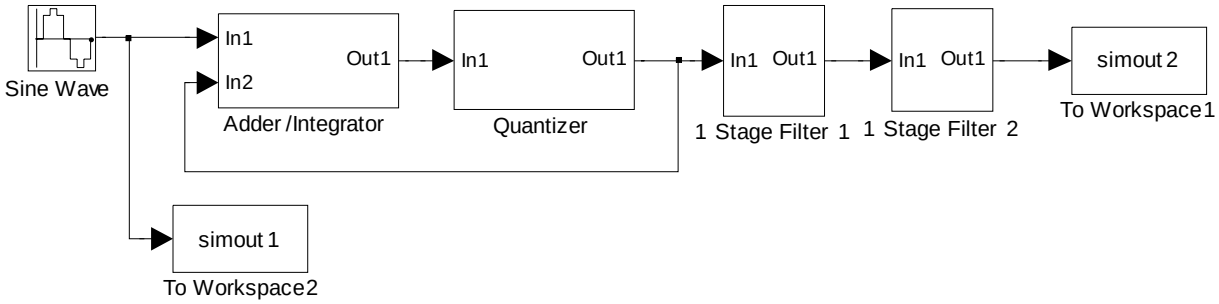

Figure 2.17 One Stage PDSM ADC Simulink Simulation Model

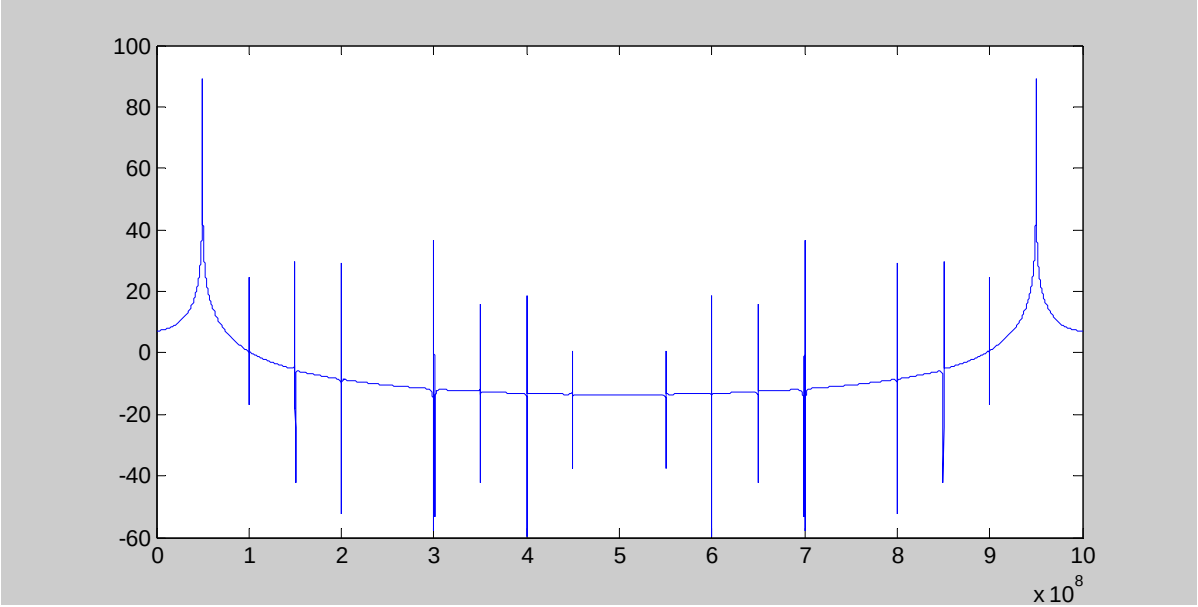

Figure 2.18

FFT Results DSM ADC 50 MHz Input without FIR Compensation Filter

The signal to noise ratio is calculated over the entire frequency range of 0 to 500 MHz and is 38.59 db. This corresponds to a resolution of 6.12 bits, which is about two bits less than with the FIR compensation filter on. It can be concluded that the proposed PDSM ADC require both SINC filter and compensation filter to get the expected resolution.

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2.4 PDSM ADC Circuit Design of 0.18um CMOS Technology

As discussed in the previous sections, to get the expected performance, the PDSM needs the compensation filter to offset the SINC filter voltage droop. The FIR compensation filter is too big to fit the minimum die size for fabrication. Since the objective is to design, fabricate and test a PDSM ADC on a minimum area die, the FIR filter compensation is not included. The details of the FIR compensation filter design can be found in reference [66].

Based on the previous discussion, a two stage PDSM ADC was designed and a transistor level circuit was captured using CMOS 0.18um technology. Figure 2.19 depicts the top level design as captured using the Cadence Analog Design Environment.

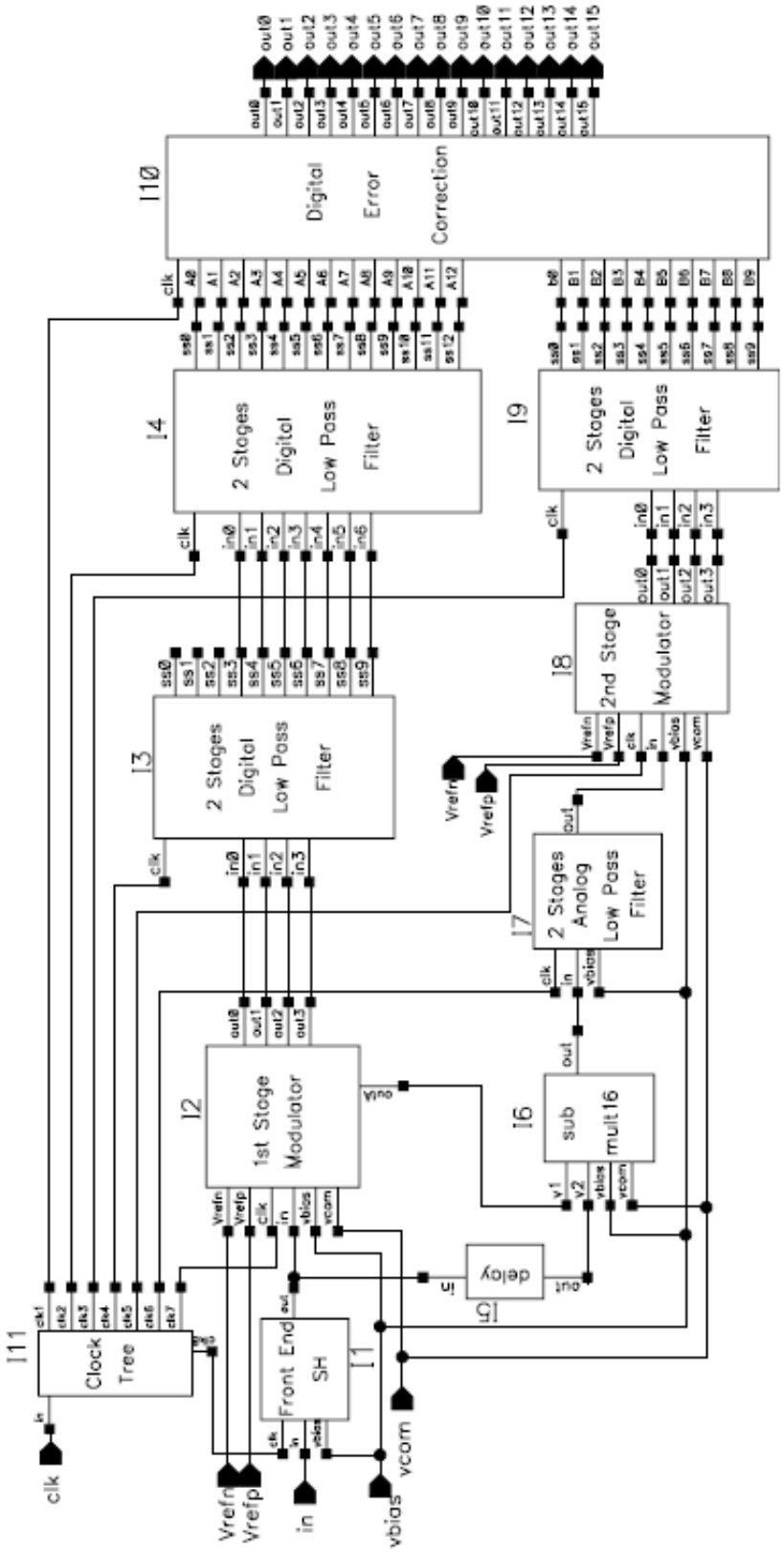

Figure 2.19 CMOS 0.18um Design for the PDSM ADC

2.4.1 Front End Track Hold Circuit

In the 4-bit flash ADC which is used in the PDSM ADC, the input is connected to 15 (2^4-1) comparators which then make decisions on the signal level in parallel. It is usually beneficial to place an S/H circuit in front of these comparators to eliminate timing or rapidly changing signal related distortion [68]. The fastest and simplest switch is a MOS switch as shown in Figure 2.20, where the C_H is the holding capacitor which can be implemented by only the parasitic capacitance for the high speed sample frequency. The advantage of single MOS switch is the simplicity and fast speed. The disadvantage is the narrow dynamic range and higher error due to the clock feed through effects. Dummy transistor can be used to reduce the feed through effects and CMOS switch can avoid the dynamic range limitations associated with single MOS switches [69].

Figure 2.21 gives a CMOS switch with dummy transistors. This switch is combined with an analog amplifier to be used as the front end sample hold circuit as labeled as block I1 in Figure 2.19. As seen in Figure 2.21, the dummy CMOS (I18) switch with input and output shorted together is clocked inversely with the switch (I16), so to mitigate clock feed through due to the normal switch (I16).

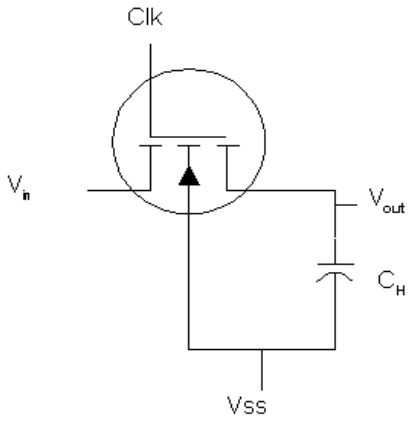

Figure 2.20 Single NMOS Switch

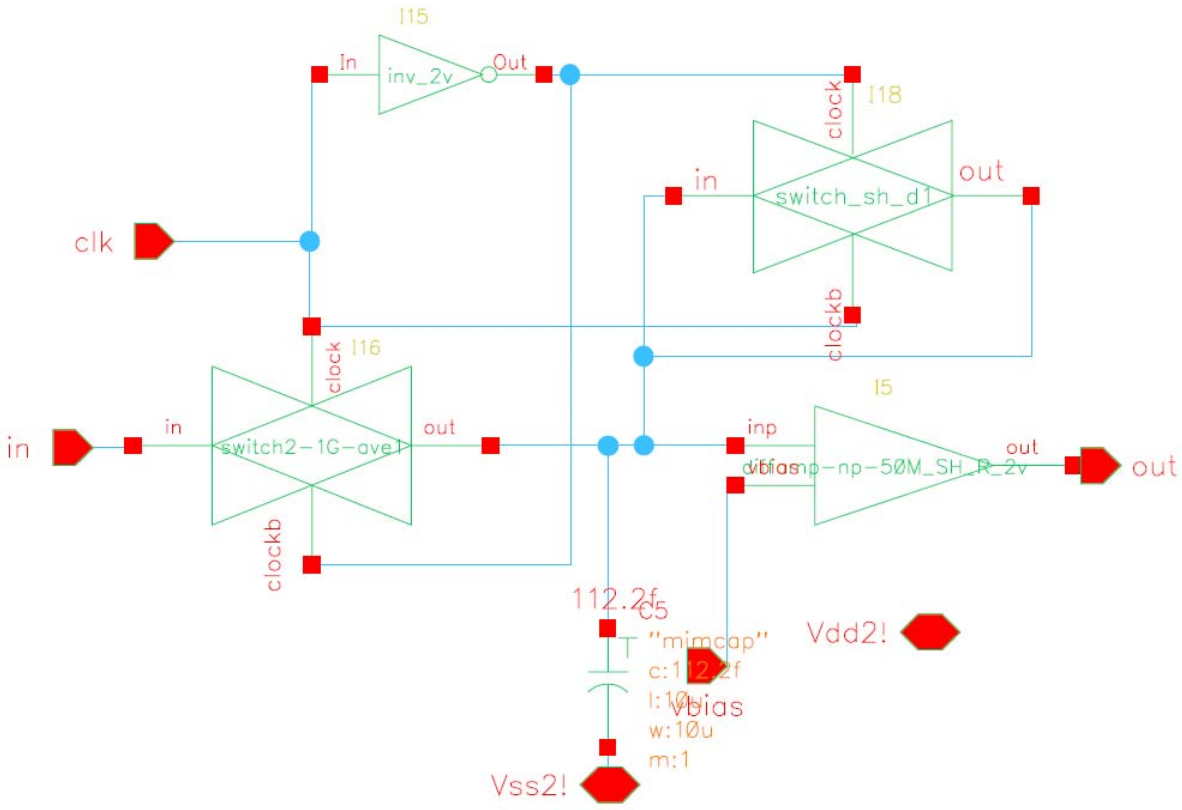

Figure 2.21 Sample Hold Block Diagram

2.4.2 Stage One PDSM ADC

Block I2 as seen in Figure 2.19 is the stage one 1st order ΔΣ modulator. The linearized model is shown in Figure 2.22.

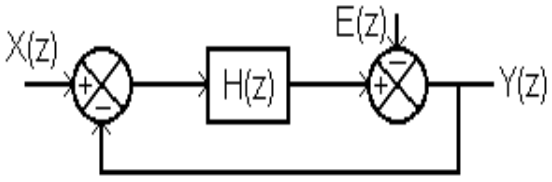

Figure 2.22 Linearized Model of First Order Delta Sigma Modulator

From Figure 2.22, it can be seen the output signal of the first order ΔΣ modulator in Z domain can be written as $Y(z) = H(z)\left[X(z) - Y(z)\right] + E(z)$

So

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z) \qquad \textbf{(2.22)}$$

Where E(z) is the quantization noise and X(z) is the input. If H(z) represents the transfer function of a discrete integrator, then

$$H(z) = \frac{1}{z-1} = \frac{z^{-1}}{1-z^{-1}} \qquad \textbf{(2.23)}$$

$$Y(z) = X(z)Z^{-1} + E(z)(1-Z^{-1}) \qquad \textbf{(2.24)}$$

Thus the signal is transmitted with one clock delay, but the quantization noise is attenuated by the magnitude of the noise transfer function i.e.

$$\left|1-Z^{-1}\right| = 2Sin\frac{\pi f}{f_S} \qquad \textbf{(2.25)}$$

Where f is the input signal frequency and fs is the clock frequency of the modulator. Thus, the noise is highly attenuated for f<<fs.

The Delta Sigma modulators are typically realized using either Switched Capacitor (SC) implementations or Continuous Time Analog Integrator (CTAI) implementations [70,71]. In this dissertation, we use a unique implementation Direct Form Integrator of a first order delta sigma modulator, which has advantages over traditional approaches, particularly for high sampling frequencies with multi-bit quantizer.

A typical SC implementation of a first order Delta Sigma modulator is shown in Figure 2.23 [70].

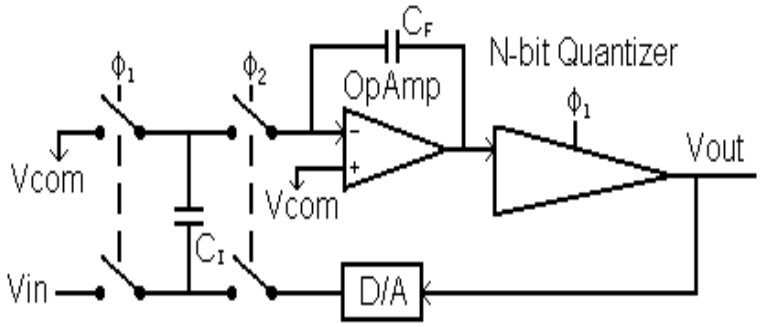

Figure 2.23 Switch Capacitor (SC) implementation of First Order Delta-Sigma Modulator

The SC implementation is efficient and the circuit will operate for a wide range of clock frequencies. However, the design is susceptible to capacitive feed through and charge injection from the analog switches which affect the accuracy of the adder and the integrator. Also the gain of the integrator (C_I/C_F) is the same for the input and the feedback signal from the D/A converter which may be restrictive for some applications. The SC implementation also requires that the quantizer and the D/A converter complete an evaluation during one phase of the clock. This can be a challenge for high clock (sampling) frequencies. Overall the traditional SC modulator is slow and the necessary capacitors are area-intensive, particularly for broadband applications with high sampling rates and relatively low over-sampling ratios [60], [72].

A typical CTAI implementation is shown in Figure 2.24. [70]

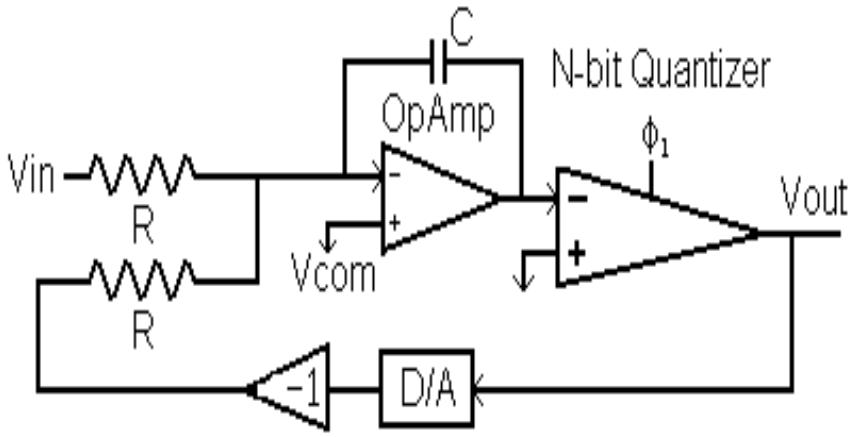

Figure 2.24 Continuous Time Analog Integrator (CTAI) Implementation of First Order Delta-Sigma Modulator

This implementation has a simple clocking scheme and is less susceptible to the clock feed through and charge injection compared to the SC implementation. One drawback is that the clock frequency must be set at the value: fs=1/(RC). Thus the clock frequency (sampling rate) cannot change once R or C are chosen. This integrator configuration also requires that fs>>f where f is the input frequency. For low over-sampling ratios (fs/2f), the transfer function of the integrator is distorted, and result in unexpected errors. Another problem is the erroneous response of the integrator to a non-ideal pulse shape of the feedback signal. This is due to the continuous time analog integration. The only clock components are the quantizer and the D/A converter, so timing constraints are not as stringent as for the switched capacitor implementation.

The unique Direct Form Integrator (DFI) implementation for the first order Delta Sigma modulator is shown in Figure 2.25.

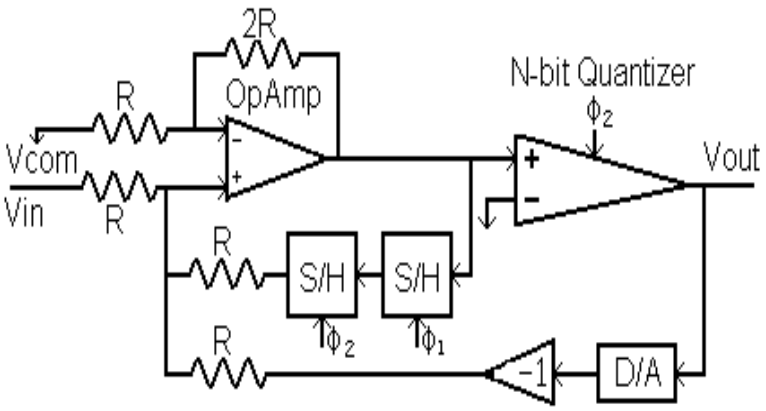

Figure 2.25 Direct Form Integrator (DFI) Implementation of First Order Delta-Sigma Modulator

A linearized model for the direct form integrator implementation is shown in Figure 2.26.

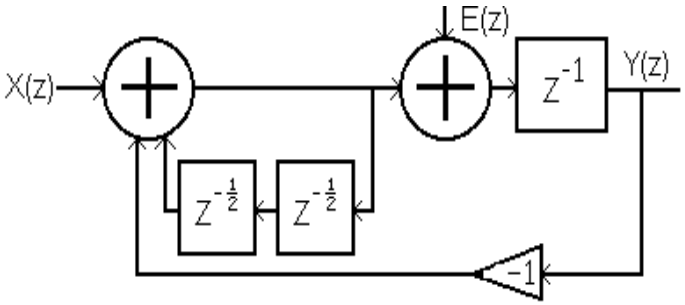

Figure 2.26 Linearized Model of Direct Form Integrator (DFI) Implementation for First Order Delta-Sigma Modulator

It is easily derived that

$$Y(z) = X(z)Z^{-1} + E(z)Z^{-1}(1 - Z^{-1}) \qquad \textbf{(2.26)}$$

which is the same as the previous implementations except the noise is delayed by one clock cycle. The quantization noise is shaped by the same function $(1 - Z^{-1})$. This design is called the direct form integrator implementation, because the integrator is realized directly as a discrete analog accumulator. This design has several advantages over both the other implementations.

- There is less susceptibility to clock feed through and charge injection, because the sample hold circuits incorporate well-known techniques to minimize these effects.
- Also, similar to the SC implementation, a wide range of clock frequencies can be used for this implementation, since the integrator transfer function does not depend on the resistor values and sample hold capacitor values. The resistor values do permit flexibility in choosing the gain for any of the adder inputs.
- Another advantage is that the direct form integrator is not sensitive to the pulse shape of the feedback signal, which is a problem for the CTAI configurations.
- A very important feature is that this design provides an edge for broadband applications with very high sampling frequencies, relatively low over sampling ratios and multi-bit quantizers. In this configuration, the output of the adder is connected directly to the quantizer. This permits a full clock cycle for the DAC, adder, and quantizer comparator operations to be completed. For a modulator using a multi-bit quantizer, this is an important advantage compared to the SC implementation where the quantizer evaluation and D/A conversion must be completed in one phase of the clock. This is particularly critical when trying to push sampling frequencies to the range of 0.5 to 1.0GHz.
- It is relatively straightforward to extend this implementation to a second or higher order modulator. The second order DFI implementation would be appropriate where higher over sampling ratios are obtained with smaller bandwidths, yielding higher resolution.

The details of the Direct-Form Integrator schematic implementation are shown in Figure 2.27 which is labeled as Block I2 in Figure 2.19.

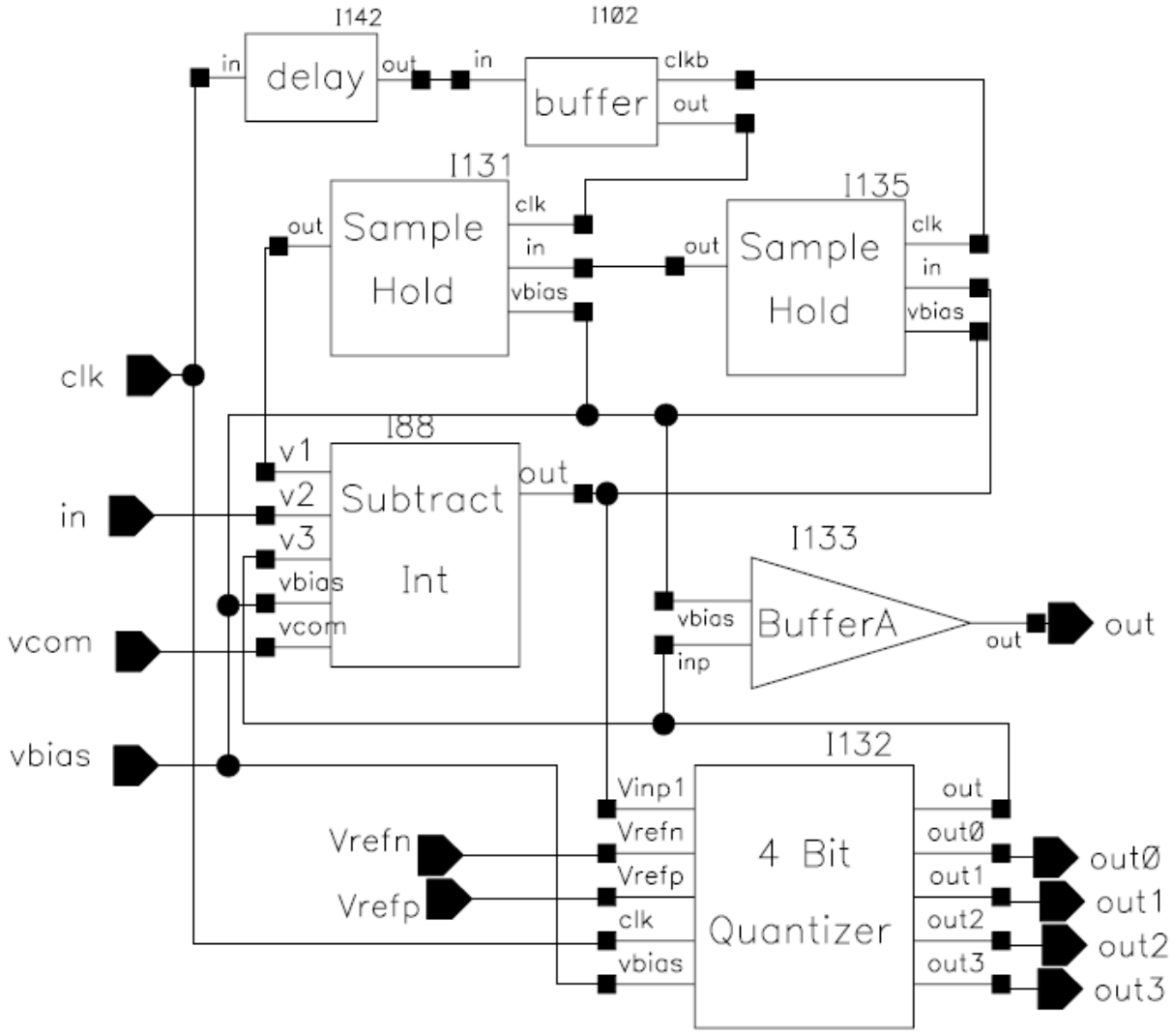

Figure 2.27 CMOS 0.18um Design for the First Order ΔΣ Modulator

As seen in Figure 2.27, the output of the integrator is fed back to the input through two sample hold circuits resulting in a Z^{-1} delay from subcomponent I88 (Subtract Int) output to the input v1. The subtract/integrator implements the discrete time integrator and also subtracts the analog version of the four bit quantizer output from the input. The analog value of the four bit digital quantiizer output is obtained from a DAC that is an integral part of the quantizer. The details of the subtract/integrator circuit are shown in Figure 2.28 which is a combination of a three input (v1, v2 and vcom) non-inverting summing

circuit with a two input (v3 and vcom) standard inverting summing circuit. The vcom input is used to set the input offset.

Base on the CMOS differential amplifier properties that the input impedance is very high, the current to both input are only leakage current which can be ignored and the voltage Vinn=Vinp=V0. So two equations can be derived:

Path v1, v2, inp to vcom **v1-v0+v2-v0=v0-vcom** **(2.27)**

Path vout, inn to v3, vcom **vout-v0=v0-vcom+v0-v3** **(2.28)**

Solve equations (2.27) and (2.28). The output voltage can be derived as equation (2.29).

Vout=v1+v2-v3. **(2.29)**

As shown in Figure 2.28, the implementation requires some fine tuning work of the on chip resistors for the desired sampled data output of the subtract/integrator to get the required resolution.

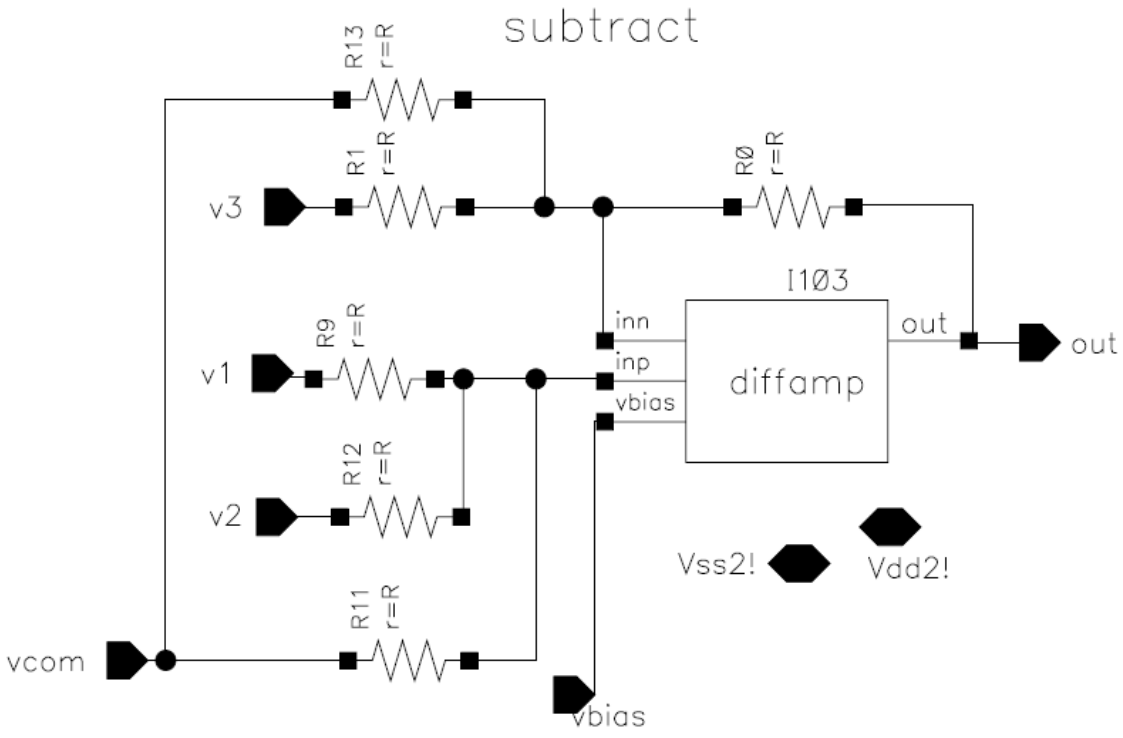

Figure 2.28 CMOS 0.18um Design Adder/Subtract for Direct Form Integrator

The 4-bit quantizer was implemented through Cadence Virtuso Schematic Composer as shown in **Error! Reference source not found.** which include a 4-bit flash ADC and a 4-bit DAC.

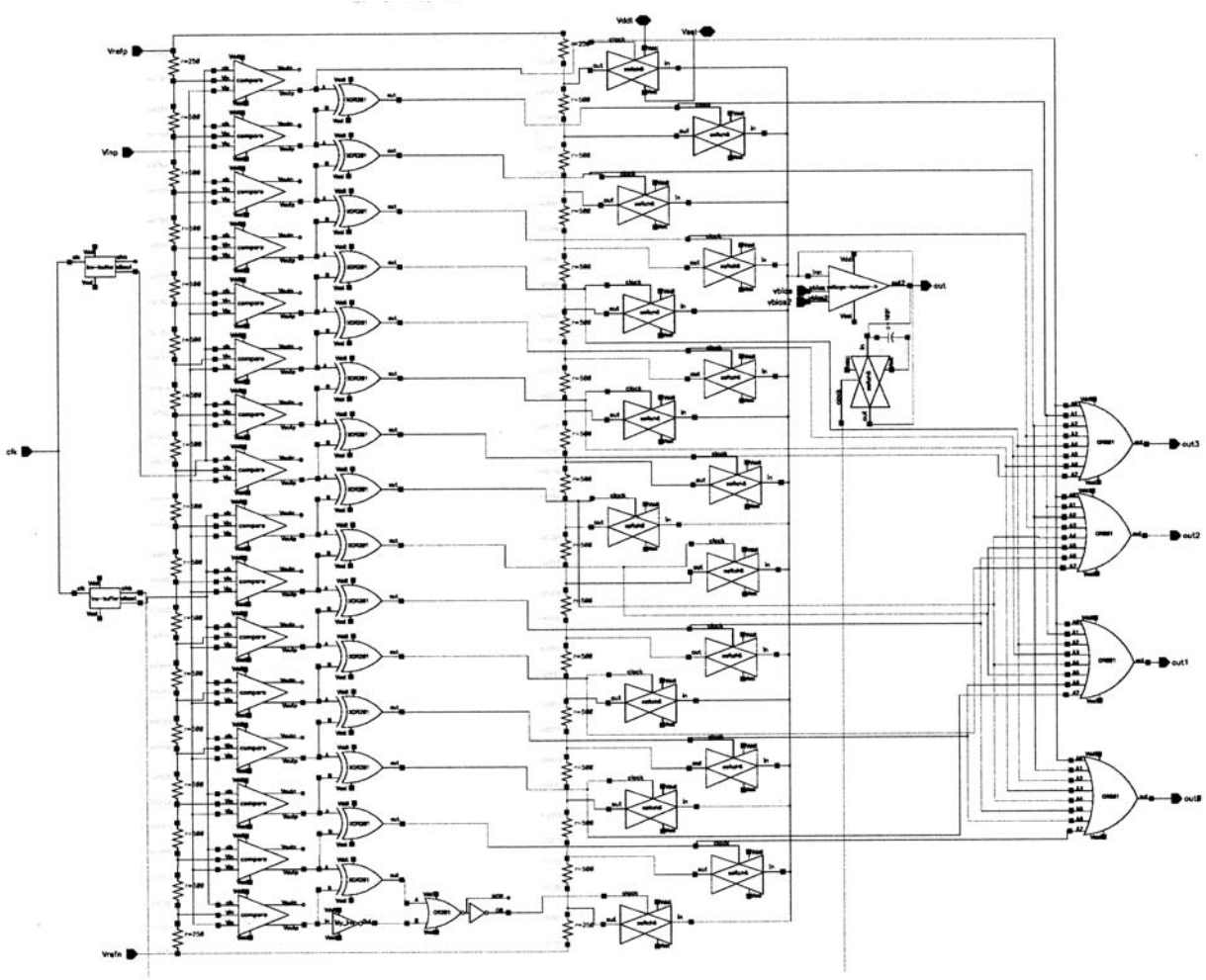

Figure 2.29 4-bit Quantizer with 4-bit Resistor String DAC

As seen in **Error! Reference source not found.**, the 4-bit flash ADC accepts an analog input from the integrator of the ΔΣ modulator, converts this to a 4-bit digital output using 15 comparators and 16 resistor network, and the 4-bit DAC which is implemented by using resistor string architecture with 15 switches and 16 resistor network, converts the 4-bit digital output to an analog feedback signal for the ΔΣ modulator. The feedback signal

becomes the third input of the integrator, v3 as seen in Figure 2.28. As discussed before, the ADC is aimed to work at 1.0 GHz sample frequency with 50 to 62.5MHz bandwidth. The feedback signal which is the analog version of the 4-bit digital output must be a stable and accurate signal to give the required feed back to the integrator. The fast changing digital bit causes glitches through the switches to the DAC and also changes the analog values through the DAC resistor tree. So for higher speed input and low over sampling ratio application, other alternative DACs could be used, such as R-2R ladder networks, charge scaling DACs [73]. A 4 bit R-2R DAC has been designed as shown in Figure 2.30 and also was integrated with the 4 bit flash ADC as shown Figure 2.31. The first order delta sigma modulator simulation results didn't show much change. As previously stated, the PDSM architecture mitigates the effect of the DAC errors and also the required DAC resolution for this application is low. Resistor string DAC was used for the final layout and fabrication only because it was investigated early.

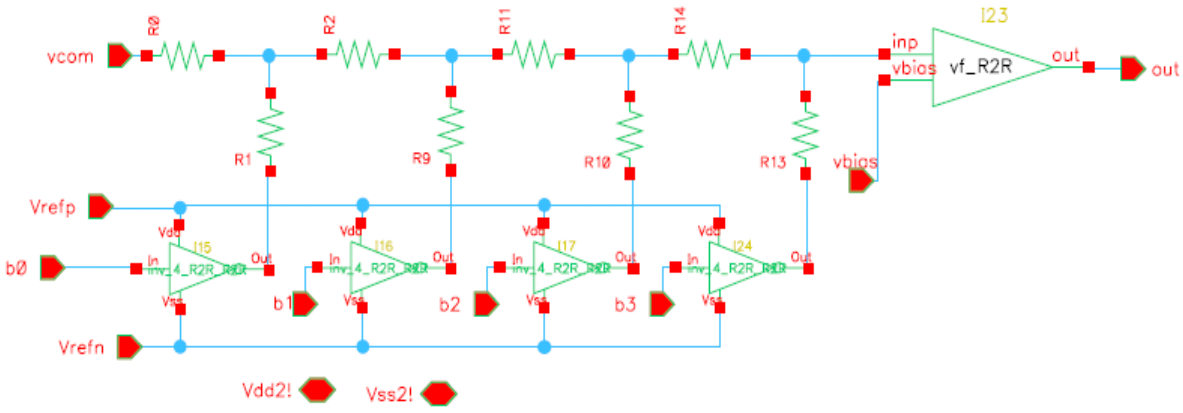

Figure 2.30 4 bit R2R DAC Circuit

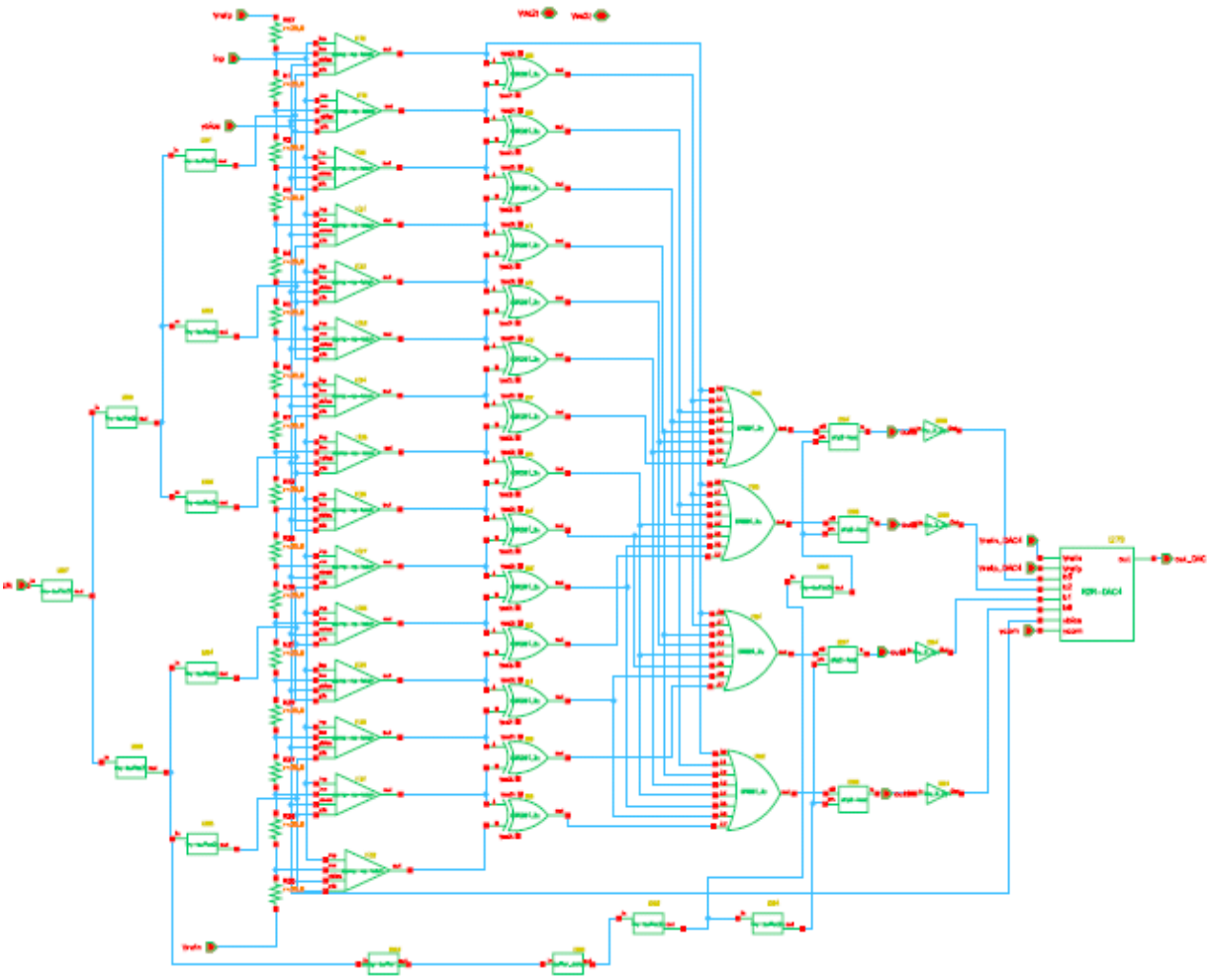

Figure 2.31 4 bit ADC with 4 bit R2R DAC

The 4 bit digital outputs from 1st stage modulator go through two consecutive two-stage cascaded digital low pass filters labeled as block I3 and I4 respectively as shown in Figure 2.19, which will be discussed later.

Custom layout for the first order ΔΣ modulator is shown in Figure 2.32 which is carefully grouped by analog and digital components. The left side of the layout, which are surrounded by the wide metals (power buses) are the analog components which include the sample holds, subtract/integrator and comparators of the quantizer. The right side of

the layout are the digital components. So two isolated pairs of power buses are used to reduce the effect of digital components on analog component operation.

Simulations have been conducted based on the extracted netlists from the layout and adjustments made to minimize the parasitic capacitance to eliminate coupling. Also metal layers were carefully selected to minimize parasitic resistance and capacitance where resistance or capacitance is a critical factor. The power buses width are calculated based on the total current and the used metal current density. The total size of the modulator is 161 um by 355 um.

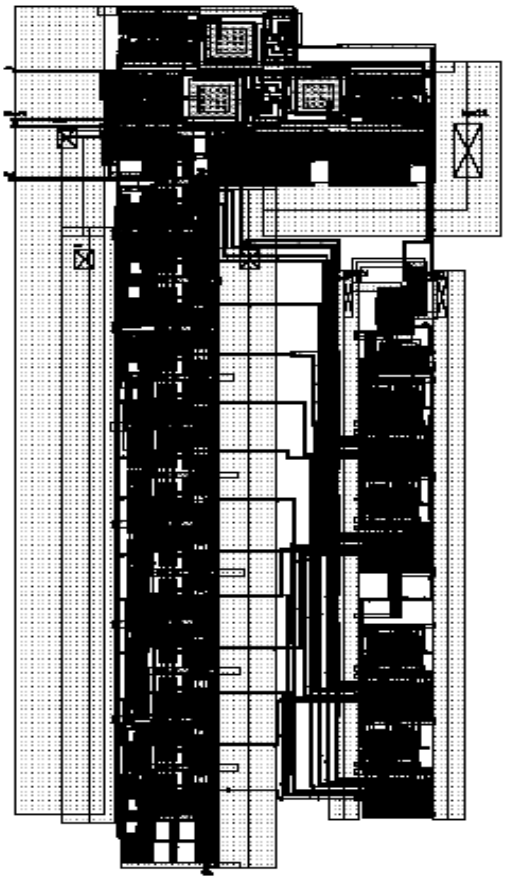

Figure 2.32 Layout of First Order Modulator for First Stage

The extracted layout simulation results of first order modulator for first stage PDSM ADC are shown in Figure 2.33, where the input is a 50MHz sine wave signal with 0.45v

amplitude and the output is the weighted sum of the four bit digital output of the modulator.

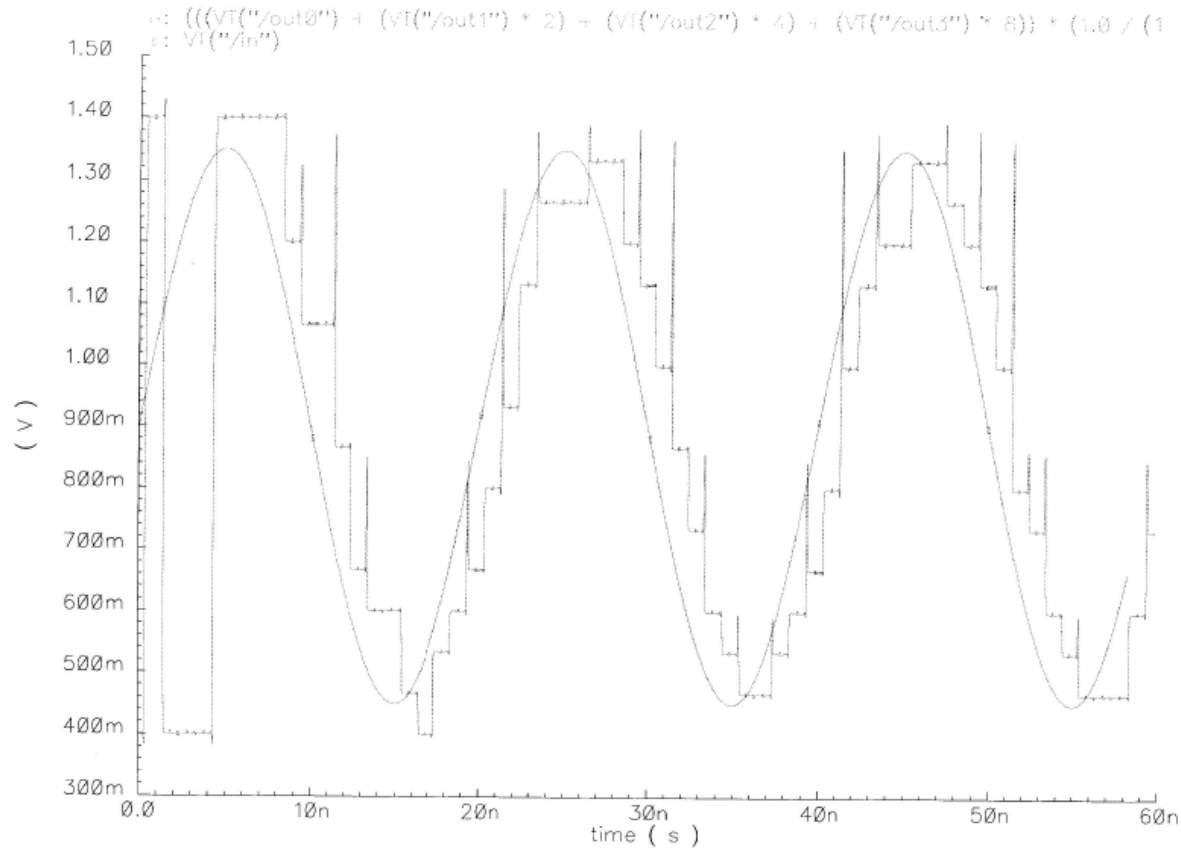

Figure 2.33 Layout Simulation Results of First Order Modulator fin=50MHz, fclk=1.0GHz

2.4.3 Stage Two PDSM ADC

As discussed above the analog signal corresponding to the first stage digital output is obtained from a DAC that is part of the first stage quantizer. This first stage analog output is an input to the subtract/multiplier circuit labeled as I6 in Figure 2.19. The function of this block is to calculate the first stage conversion error and amplify this error with the proper gain to generate an input to the 2nd stage 1st order ΔΣ modulator. The error signal is derived by subtracting the first stage analog output from the sampled data

input signal (delayed by one clock to match the delay of the first stage analog output). The one clock cycle delay on the input is obtained by a cascade of two sample hold circuits similar to that used in the direct form integrator discussed previously. Some details of the subtract/multiplier circuit, which has two stages of amplifiers [74], are shown in Figure 2.34. As seen in Figure 2.34, the first stage of the subtract/multiplier circuit is a differential input/differential output amplifier. The differential output is the difference of the two inputs with certain gain. The second stage of the subtract/multiplier circuit is a differential input/single ended output amplifier. The total gain of this circuit is

$$\text{Gain} = \left(\frac{2R1}{R0}+1\right)\frac{R6}{R5}\ , \quad \text{where R6=R4, R5=R3, R1=R2.} \qquad \textbf{(2.30)}$$

So the output of the multiplier is $Vout = (v1 - v2) \times \left(\frac{2R1}{R0}+1\right)\frac{R6}{R5}$

Proper selection of resistors gives a gain of 16 which is consistent with the four bit output of the first stage. The buffer is used to isolate the subtract/multiplier with the following subsystems and also to get driving load capability.

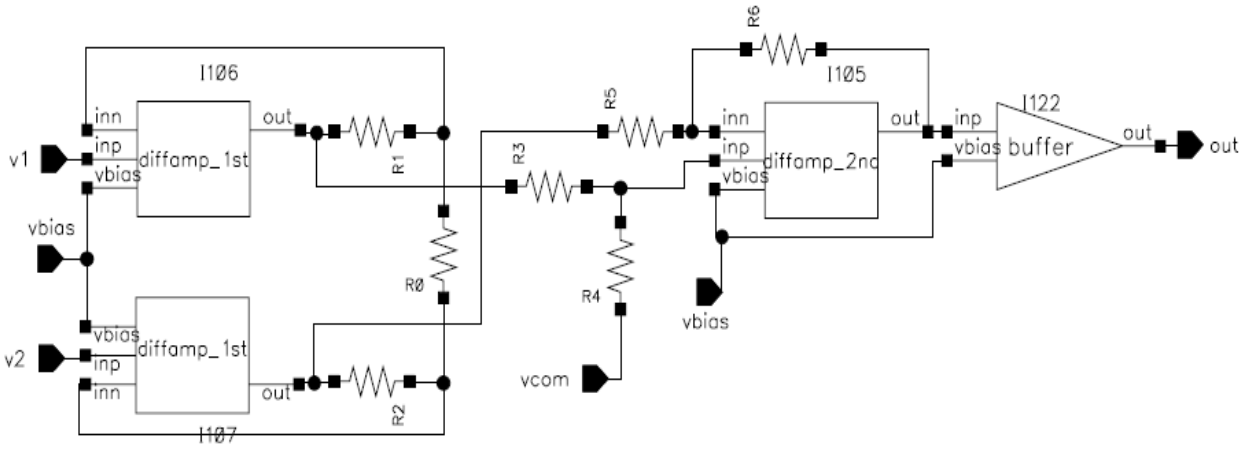

Figure 2.34 CMOS 0.18um Design of Subtract/Multiplier Circuit

The amplified analog error signal is the input to a two stage analog averaging filter labeled as I7 in Figure 2.19. The analog averaging filter is a key feature of the design and

will be discussed in the following section. The output of the averaging filter is connected to another amplifier with gain of 4. The first stage error signal amplified by 64 is the input of second stage 1st order ΔΣ modulator as labeled block I9 in Figure 2.19. Block I10 in Figure 2.19 is the digital correction/combination circuit to obtain a 16 bit digital output. All components, including track/hold, analog and digital filter can be clocked up to 1.2 GHz. The total number of transistors for the two stage design is approximately 40,000. The dynamic range of the input is 0.9 volt peak to peak for a 1.8 volt power supply.

2.4.4 Averaging filter

A key feature of the PDSM ADC architecture is the averaging technique [48] which combines delta-sigma modulator over sampling concept with an averaging technique to reduce the accuracy requirements of the analog sample hold circuits, the first stage DAC, and the subtract/multiplier, and also reduces the effects of component mismatch induced errors [82], [75]. The analog averaging filter should have the same transfer function as the digital filters at the output of the first stage, so that the first stage output and the second stage error output have been subjected to the same total transfer function. That is the analog averaging filter has the same transfer function as one of the digital filters for the first stage, which is a cascade of two SINC filters ($Sinc^2$). Note that the analog averaging filter is possible because of the over sampling; thus several samples can be averaged without losing information in the signal bandwidth.

2.4.4.1 Analog Averaging Filter

The two cascaded analog averaging filter is designed as shown in Figure 2.35 with the proper control logic implemented by clk_generator1 and clk_generator2.

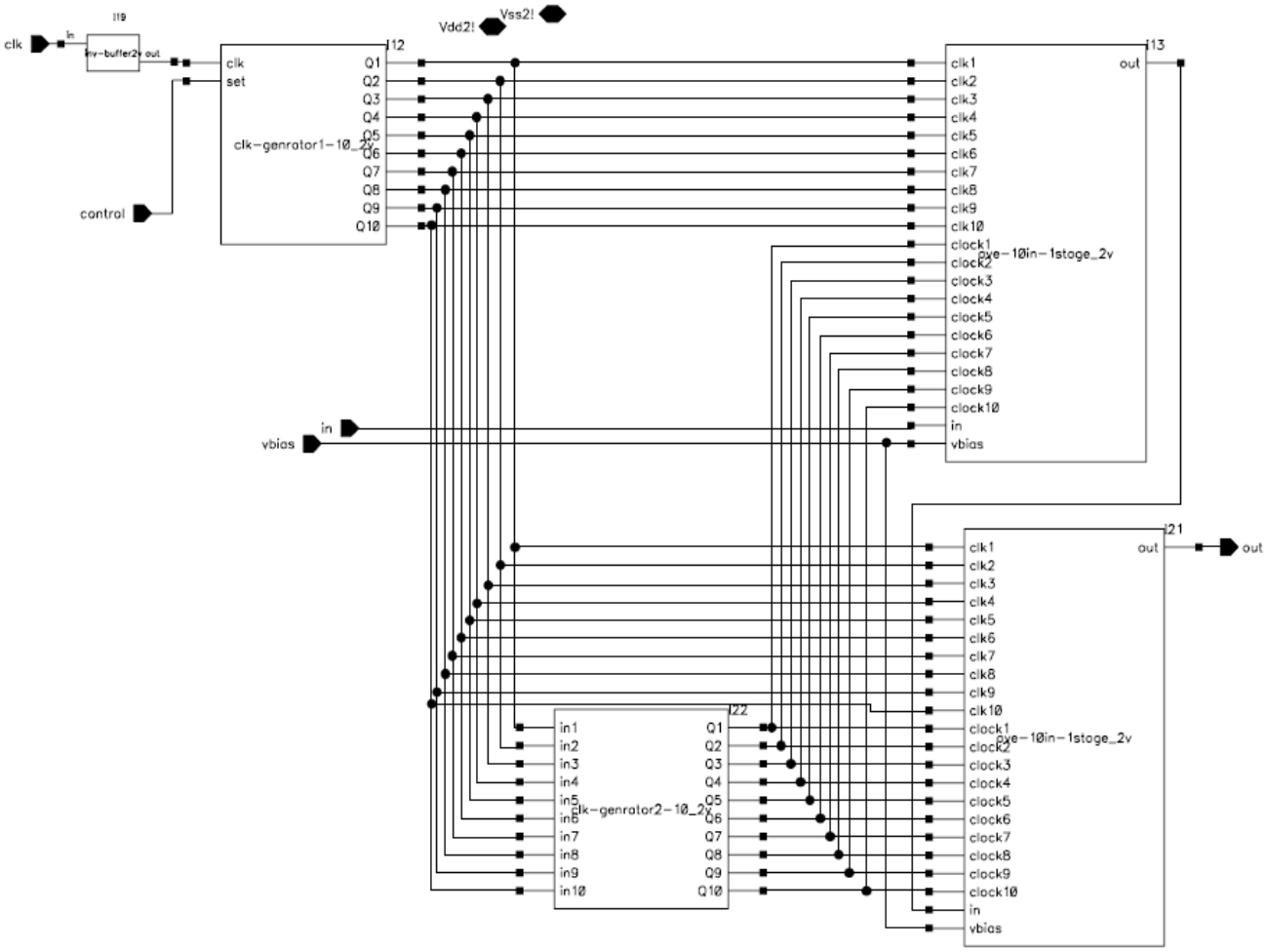

Figure 2.35 CMOS 0.18um Design for two stage analog filter

Each single stage filter has 10 sample hold circuits with same input and 10 pass gate switches as shown in Figure 2.36 which permit the averaging of 8 signals at any time while in the hold state.

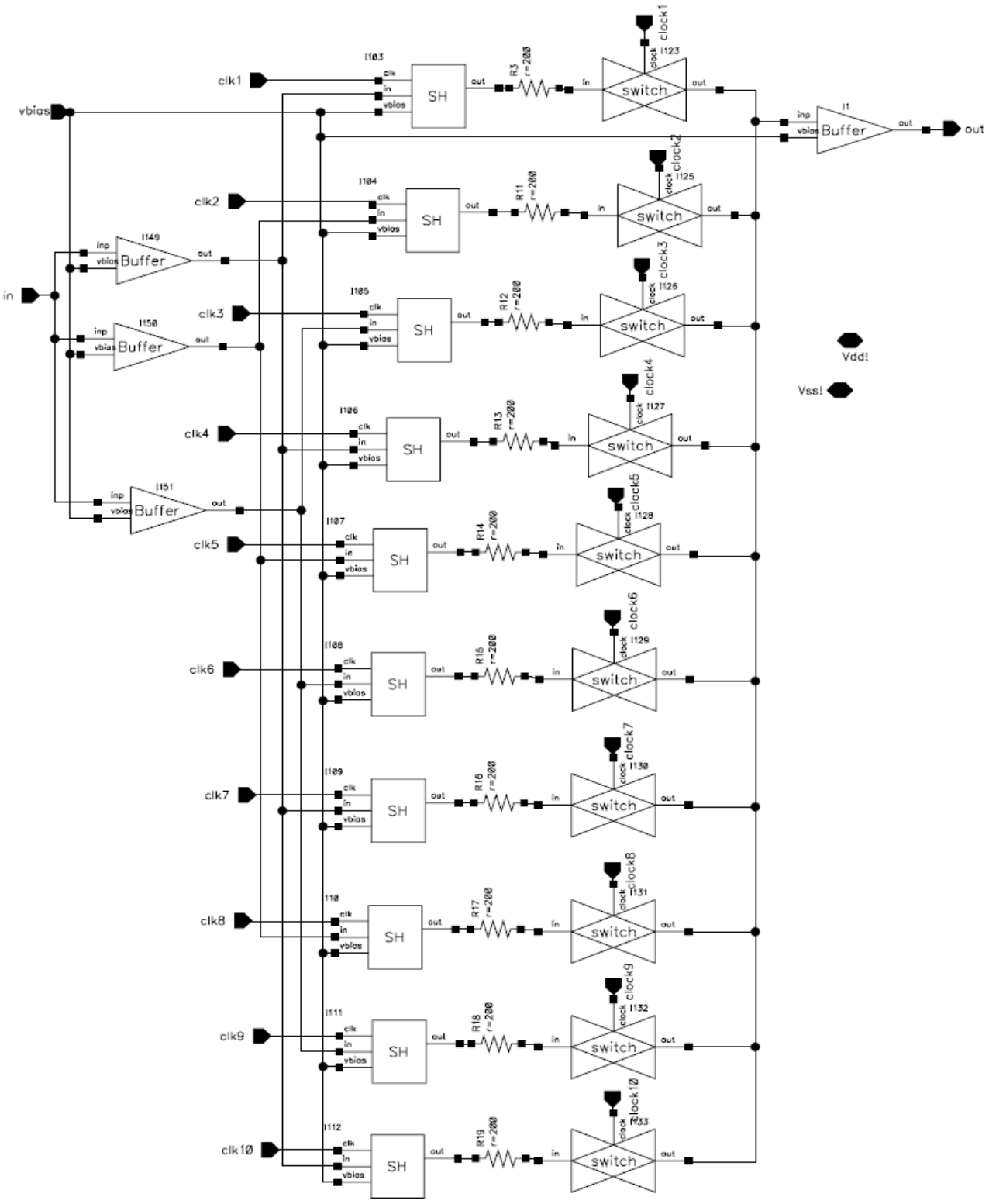

Figure 2.36 CMOS 0.18um Design for Single Stage Analog Filter

As seen in Figure 2.36, the three front end analog buffers were added to keep any consecutive sample hold from feeding back to each other. The control logic signals are shown in Figure 2.38. As seen in Figure 2.38, Clk1 is the clock control signal of sample hold 1 (the top one) in the analog averaging filter; clk2 is the clock control of sample hold2 and so on. Each clk signal has a 2 cycle pulse width and 10 cycle period; so each sample hold would have a 2 cycle tracking time and 8 cycle holding time. Any two consecutive sample hold circuits would have one period of overlap tracking time, so three front end buffers are needed so that no front end buffer has the output going to adjacent (consecutive) sample holds. Following each sample hold, a pass gate switch is added to control the output sequence of each sample hold signal as shown in Figure 2.39; the control signals are labeled as clock1, clock2, … clock10 which are the inverse of each related sample hold control signal. It indicates that the sample hold signal will be read out during the holding mode which last 8 cycles. As seen in Figure 2.40, at any time, there will be 8 sample hold signals shorted to the output through the analog filter switch control as shown in Figure 2.36 to the generate average output

$$out = \frac{1}{8}\sum_{i=1}^{8} Vin(i) \qquad \textbf{(2.31)}$$

to cancel the sample hold feed through. For this 1 GHz frequency application, each sample hold will have 2ns tracking time and 8ns holding time. Each control signal is delayed by 1ns with respect to its previous one and has a pulse width of 2ns, and a period of 10ns. Figure 2.36 gives the detail circuit design of one stage analog filter. Figure 2.37 is the clock generator for 10 sample hold circuits. The generated waveform as discussed above is shown in Figure 2.38. The clock generator 2 generates the clocks for the pass

gate switches which the circuit is shown in Figure 2.39; the generated waveform is shown in Figure 2.40. It can be seen the clock 2 is just the inverted clock 1.

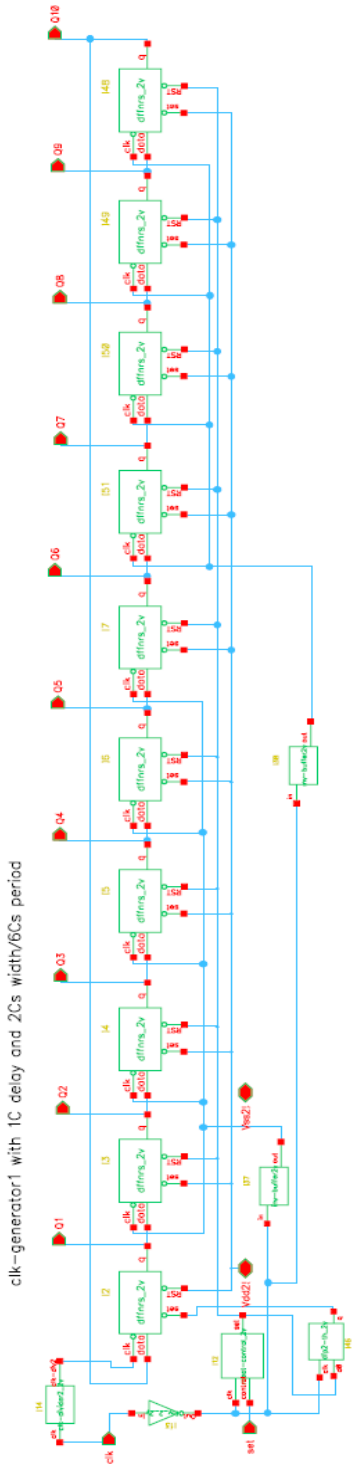

Figure 2.37 Clock Generator Circuit One

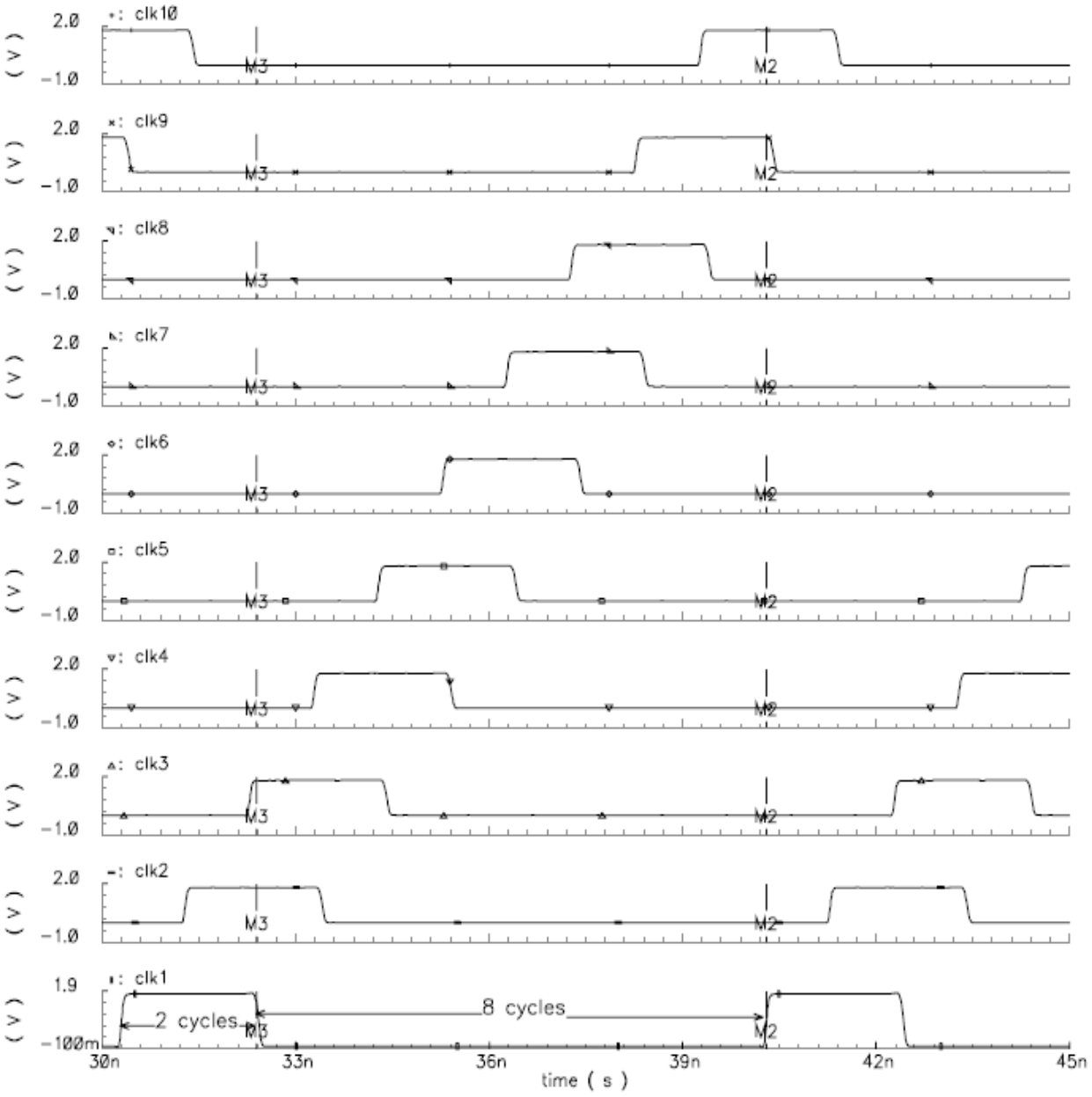

Figure 2.38 The Control Logic for 10 Sample Hold in Analog Filter

Each control signal has 10 cycles period and 2 cycles pulse width;

Each next control signal is propagated one cycle and has one cycle pulse overlap with the previous one

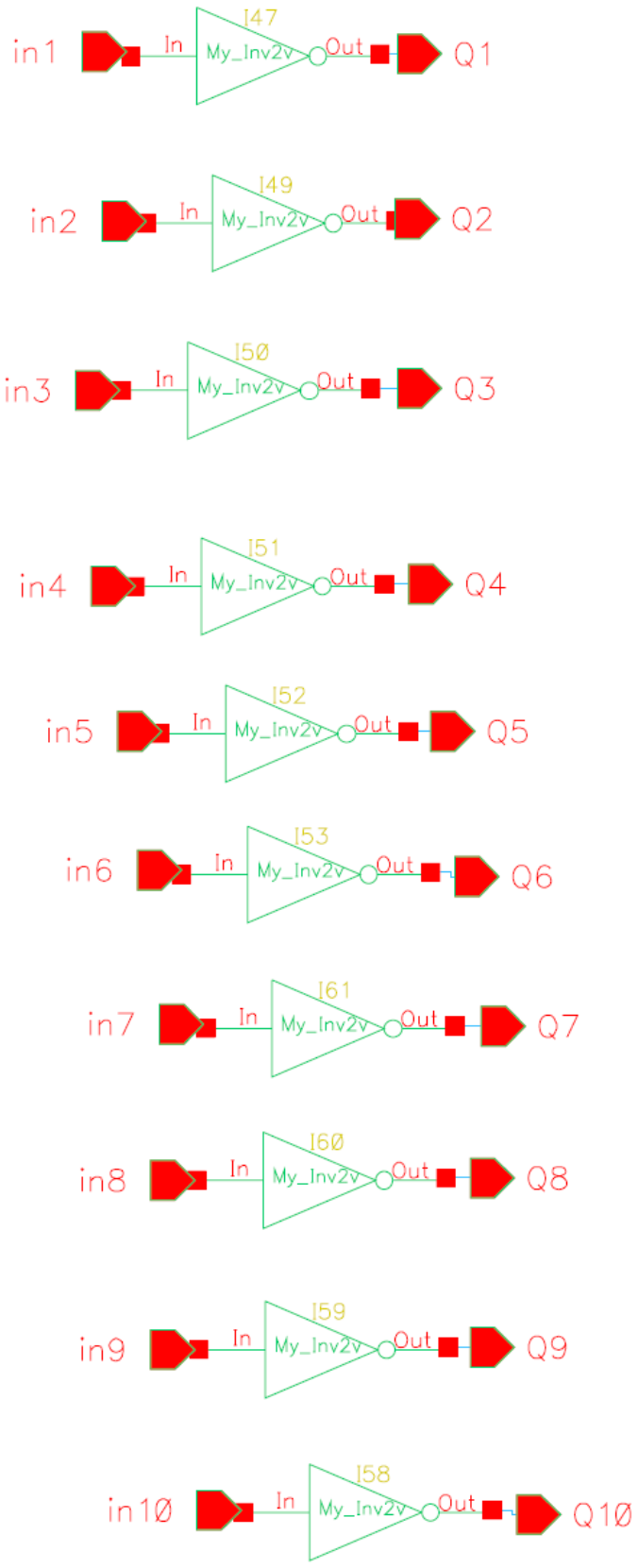

Figure 2.39 Clock Generator Circuit Two

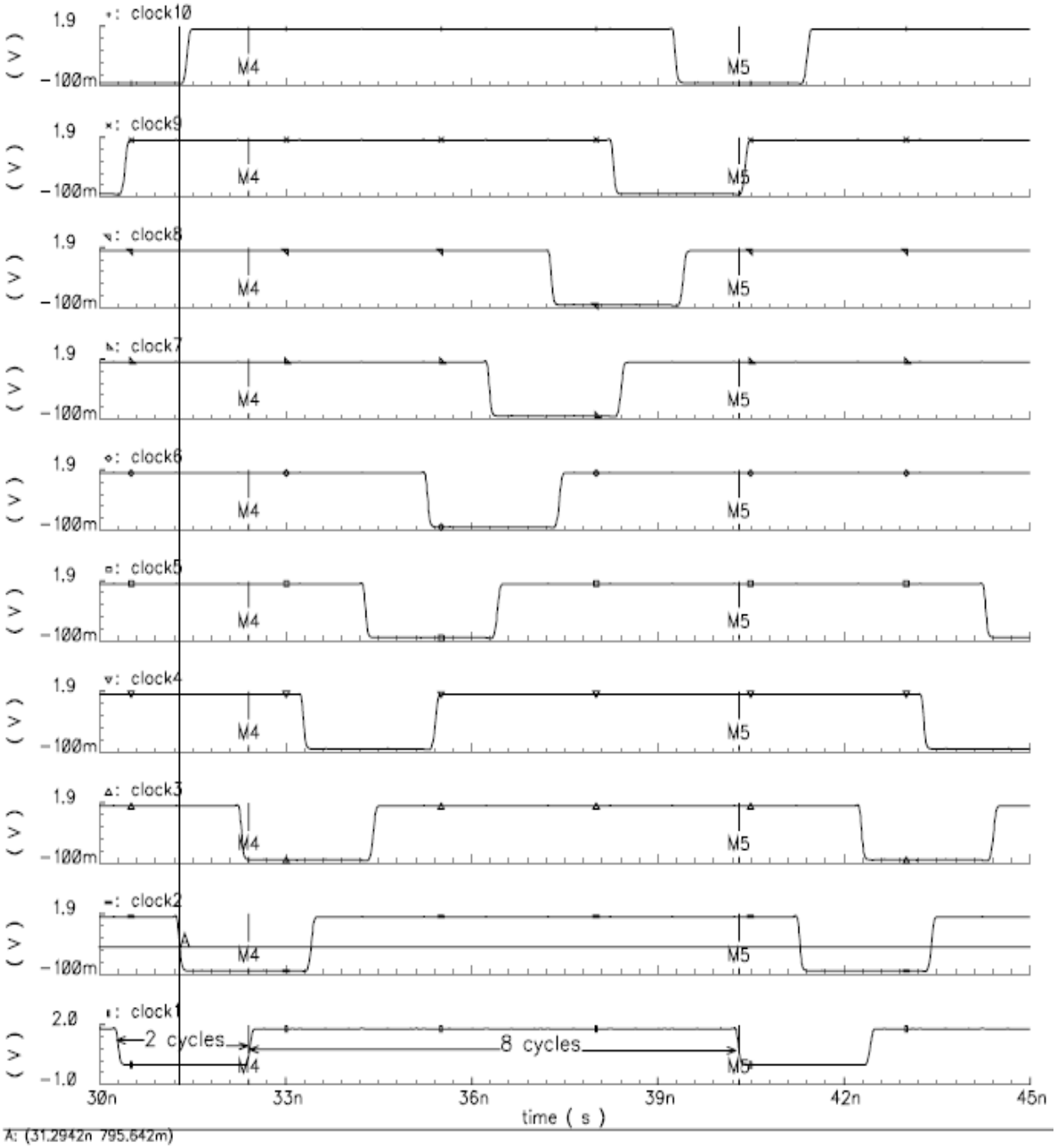

Figure 2.40 The Control Logic for 10 Pass Gate in Analog Filter
Each control signal has 10 cycles period and 8 cycles pulse width

The analog average subsystem in Figure 2.35 has been captured as a completed layout. The layout is shown in Figure 2.41 below. Adjustments were made to minimize coupling

capacitance and resistance which include avoiding any two consecutive metals cross each other and reducing the metal overlapping. After several iterations, the simulations based on layout and schematics are comparable. The size of this subsystem is 351um by 465um.

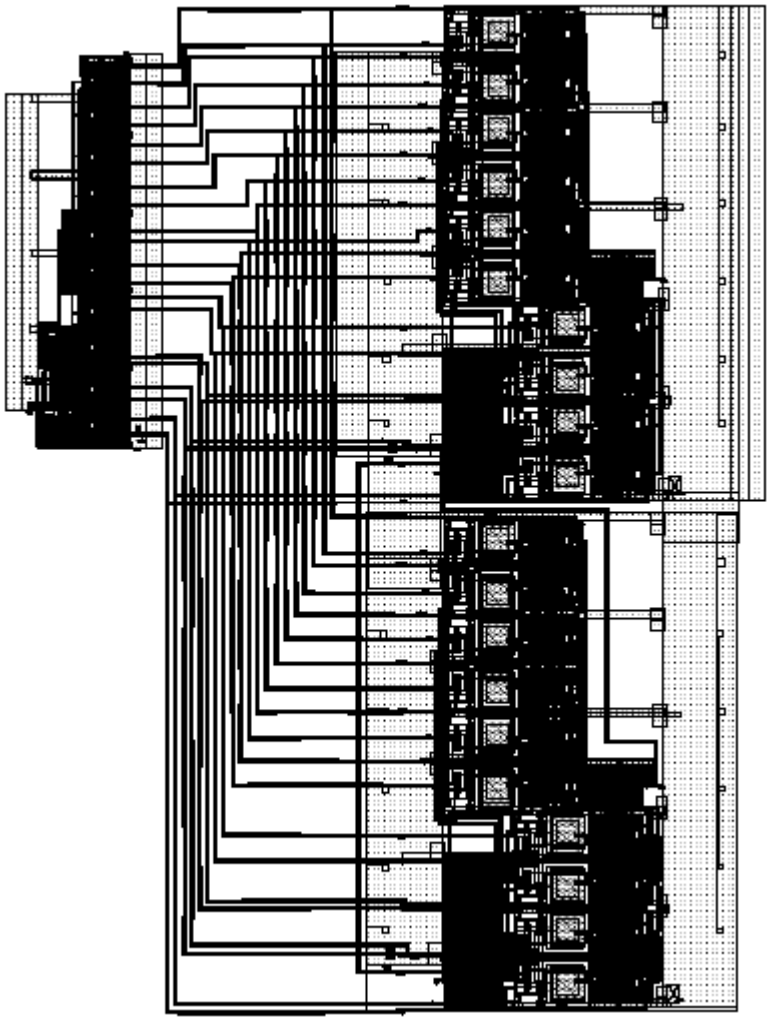

Figure 2.41 Layout of the Two Stage Analog Average Subsystem

Figure 2.42 shows the two stage analog average layout simulation results with 50MHz input and 1.0GHz sample frequency. As seen in Figure 2.42, the two bigger signals are the input signal decimated by 1/0.93935 and the first stage averaged output respectively; the two small signals are the input signal decimated by 1/0.759948 and the second stage

averaged output respectively. The coefficient 0.93935 and 0.759948 are single stage and two cascaded stage SINC filter amplitude droop factor respectively.

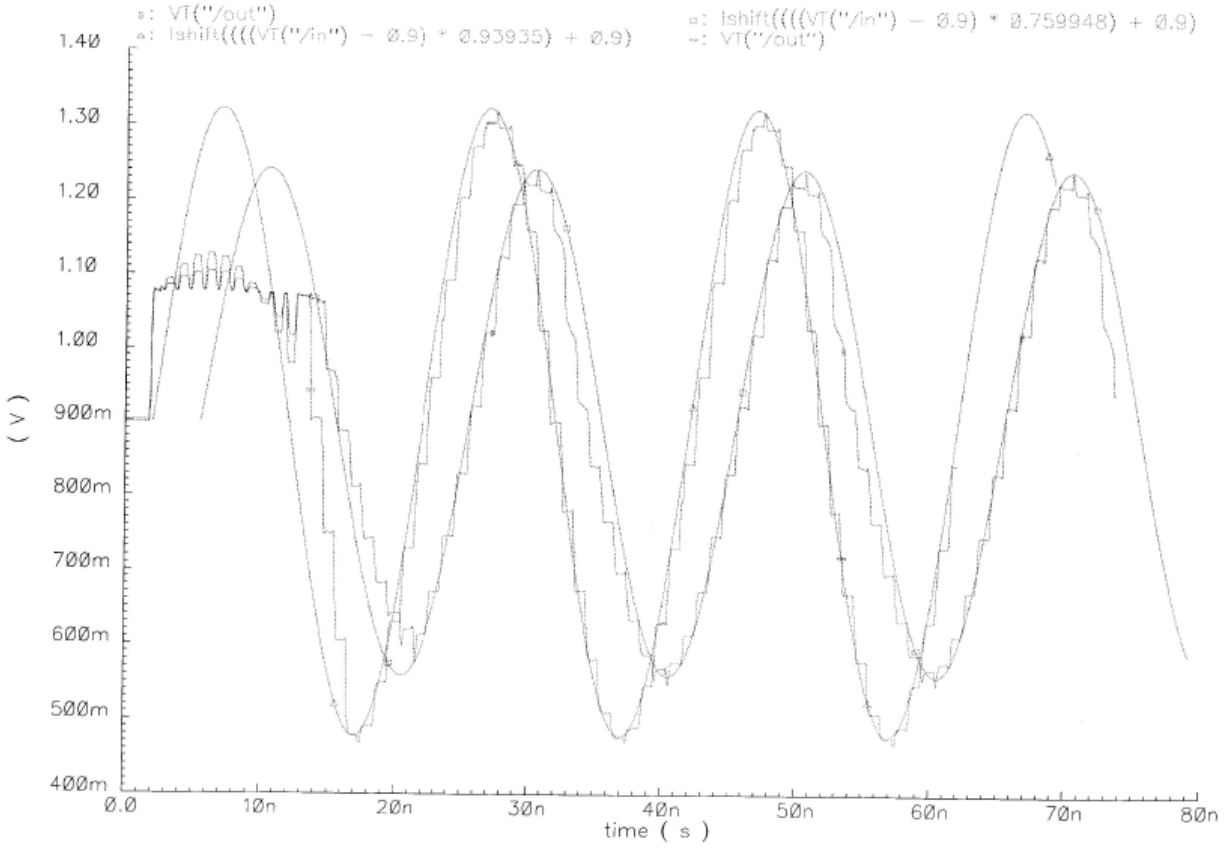

Figure 2.42 Layout Simulation Results of the Two Stage Analog Average Circuit

2.4.4.2 Digital Averaging Filter

1. Two Stage Digital Low Pass Filter Design

As discussed in the previous MatLab section. The digital average technique is implemented by using digital low pass filter.

Figure 2.43 shows the four bit digital averaging filter implementation block which is a Wallace tree adder structure to the average function $T_{ave}(z) = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i}$.

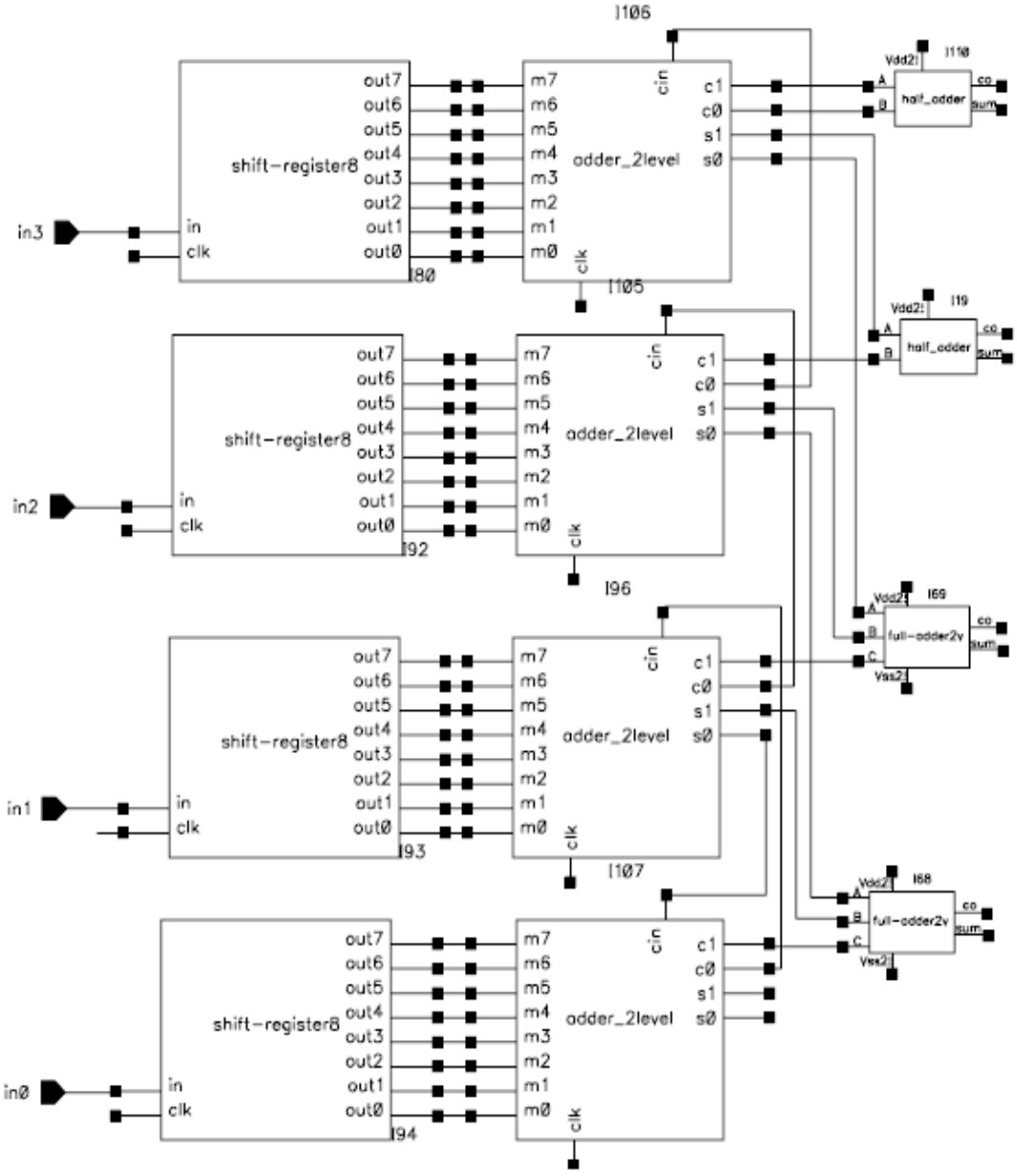

Figure 2.43 4 Bit Digital SINC Filter Design Block

The length M of the filter is 8, so each input signal will go through 8 registers to get 8 shifted signals as shown in Figure 2.44. As seen in Figure 2.44 the eight shifted output signals are labeled as “out0”, “out1”, … and “out7’ from top left to top right. The input is on the right of the circuit, which is labeled as “in”. The clock is on the bottom right which drives two clock tree buffers. Each buffer drives four registers. Each output has

one more clock cycle delay compared to its previous one, such as out0=in(z^{-1}), out1=in(z^{-2}), out2=in(z^{-3}), …. Out7=in(z^{-8}), where 'in" is the one bit digital input signal.

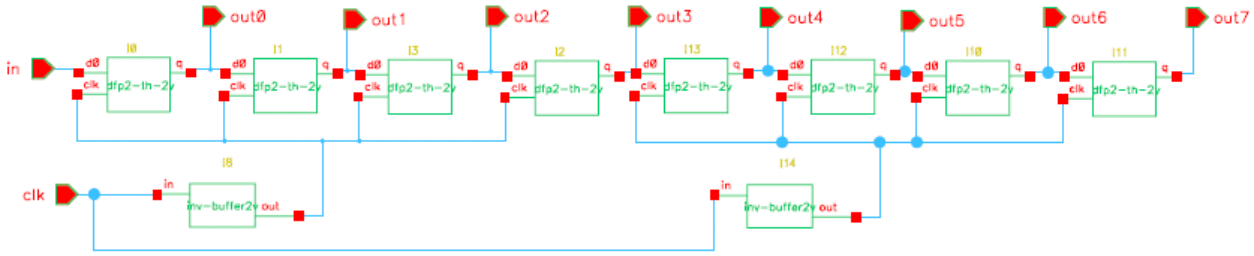

Figure 2.44 8 Shifter Registers to Generate the 8 Delayed Signals

The 8 shifted signals from each shift register will go to a carry save summing circuit as shown in Figure 2.45 to do the averaging sum function and generate two summing outputs (s0, s1) and two carry outputs (c0, c1).

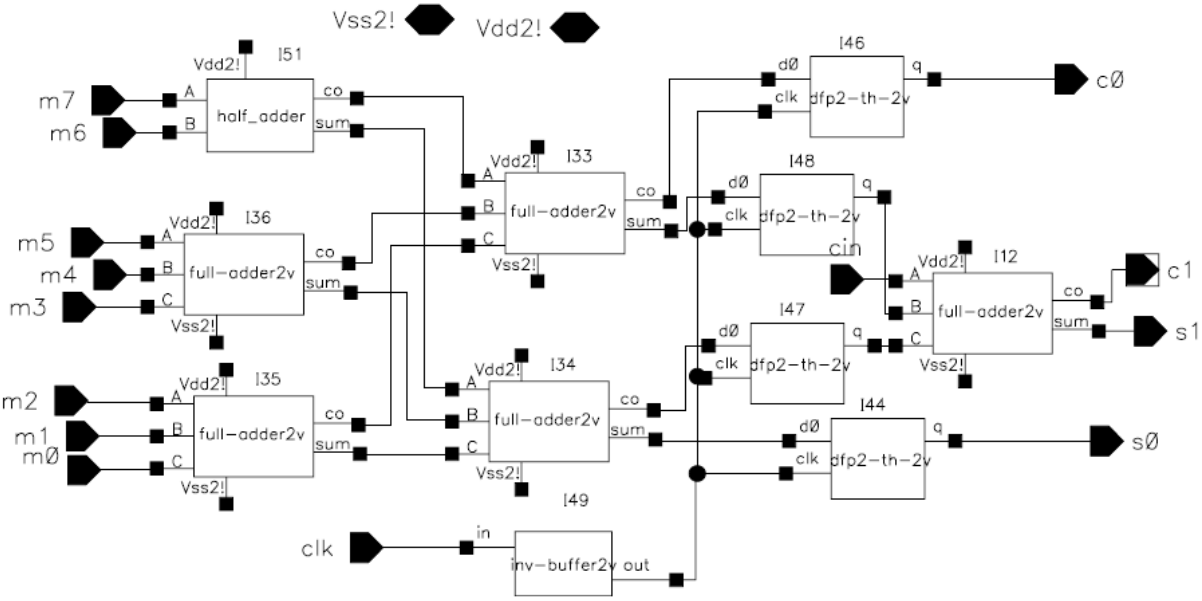

Figure 2.45 Carry Save Summing Average Circuit

As seen in Figure 2.43, the output of the 8 input summing average circuits for each of the digital bits are then combined with half adders and full adders with the proper weight to implement the first stage of the two stage SINC averaging filter. The critical design for

the digital filter is to optimize the critical path, each component size and set the proper pipelined to make sure both the layout and schematic circuit would work under the worst digital input data. It is always better to give some extra time space than just work at the edge, but it's a tradeoff between the power and the speed. The more pipeline the circuit has, the fast of the operation, but more power and more hardware will be consumed.

The test circuit for checking the two stage digital low pass filter is shown in Figure 2.46.

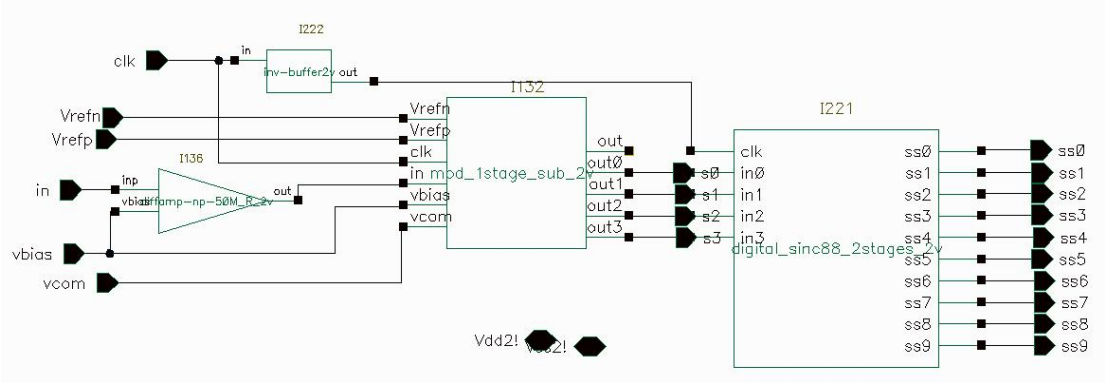

Figure 2.46 Test Circuit for Two Stage Digital Low Pass Filter

The test circuit in Figure 2.46 includes a front end buffer, a first stage delta sigma modulator with the four bit digital output of the modulator as the input to the two stage digital low pass filter. The output of the first stage of the filter is a 7 bit digital signal and the output of the second stage filter is a 10-bit digital signal as seen in Figure 2.47 below.

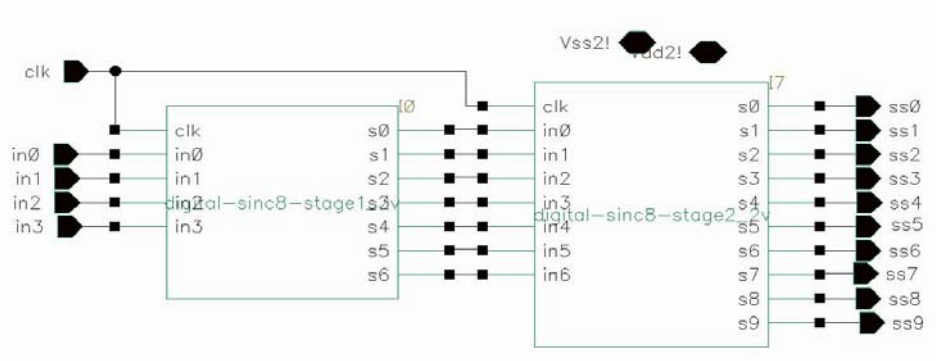

Figure 2.47 Two Stage Digital Low Pass Filter

Figure 2.48 gives the first stage digital filter top level schematic circuit, which has four digital inputs In0 to In3 (from bottom to top) of the left side and seven digital outputs out0 to out6 (from bottom to top) of the right side, where In0, out0 represent input and output Least Significant Bit (LSB) respectively, In3, out6 represent input and output Most Significant Bit (MSB) respectively.

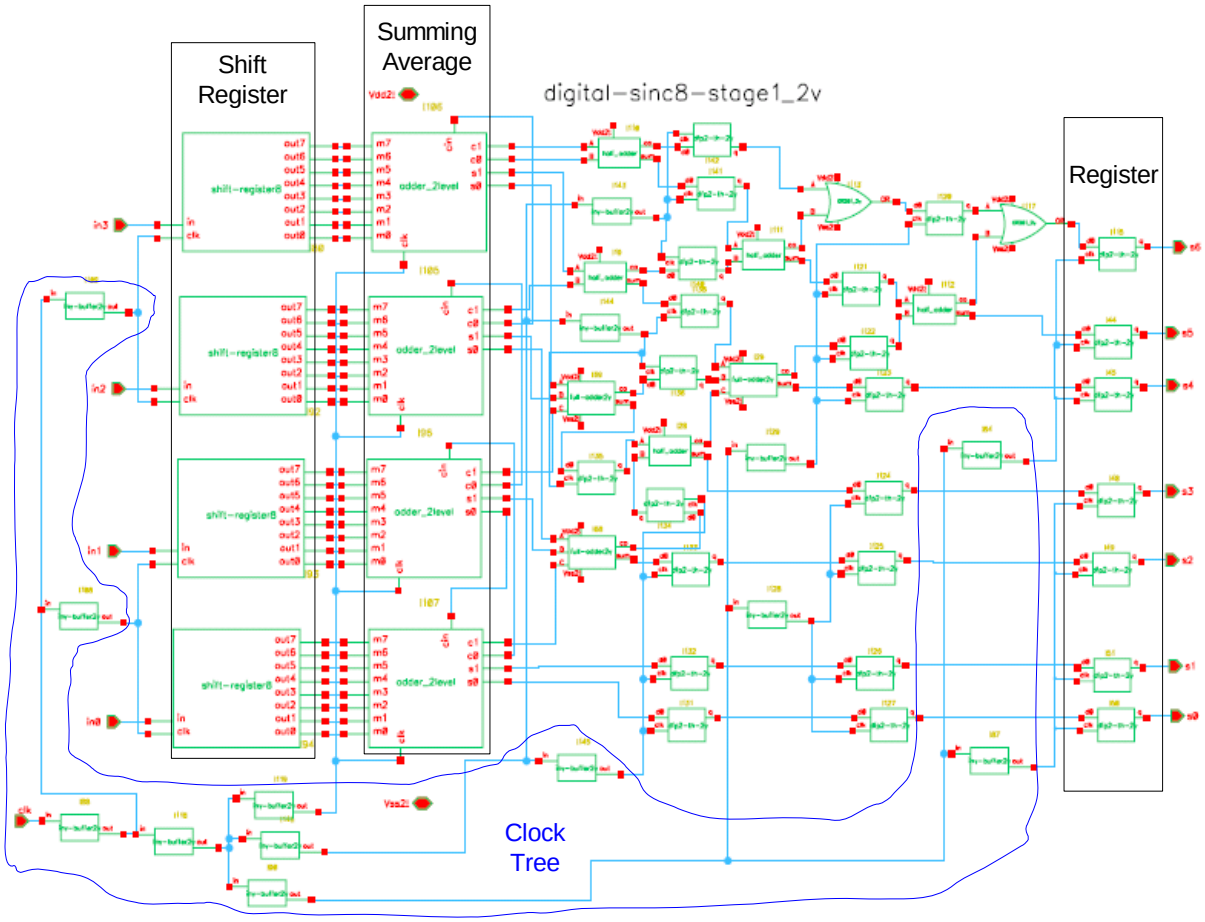

Figure 2.48 First Stage Digital Filter Top Level Schematic Circuit

As seen in Figure 2.48, the four bit digital signals of the first order delta sigma modulator go through four 8-shifter registers and four summing average circuit as discussed above. Each summing average circuit generates four outputs which are labeled as s0, s1 and c0, c1. Again referring to Figure 2.48, if we label the bottom summing average subsystem as

block1, the above one as block2, the next above as block3, the top one as block4, then the total 16 output of the these four summing average circuits can be named as s10, s11, c10, c11; s20, s21, c20, c21; s30, s31, c30, c31; s40, s41, c40, c41. To finish the SINC filter function, the following logic circuits are used:

- Connect signal c10 to block 2 cin, s20 to block 1 cin, c20 to block 3 cin, c30 to block 4 cin.
- S10 and s11 are the least two significant of the filter, which pass through two cascaded registers and go to the final register directly.
- The rest signals are combined with two full adders 1) c11+s21+s30, 2) c21+s31+s40 and two half adders 1) s32+s41, 2) c40+c41.
- The sum of the first full adder becomes the third least significant bit of the filter and the carry goes up to combine with other signals. The rest logics are straight carry save adder logic.
- The clock frequency is 1.0GHz. To keep the circuit operate correctly, each logic path delay has to be less than 1ns. For the longest path of six adders, it is very difficult to have the function done in 1ns with CMOS 0.18um technology. So two pipelined registers are used for this carry save adder structure.

As seen in Figure 2.48, except the shift register block, summing average and carry save adder block, it also includes a final register block to synchronize the entire output for the following subsystem to use and a clock tree circuit to supply all the clocks for the subsystem with the appropriate delay and driving buffer.

Figure 2.49 shows the second stage digital filter top level schematic circuit. The basic architecture is the same as first stage filter, but the input is 7 bit signals out of the first

filter and the output becomes 10 bit. The circuit is becoming bigger and more complicated

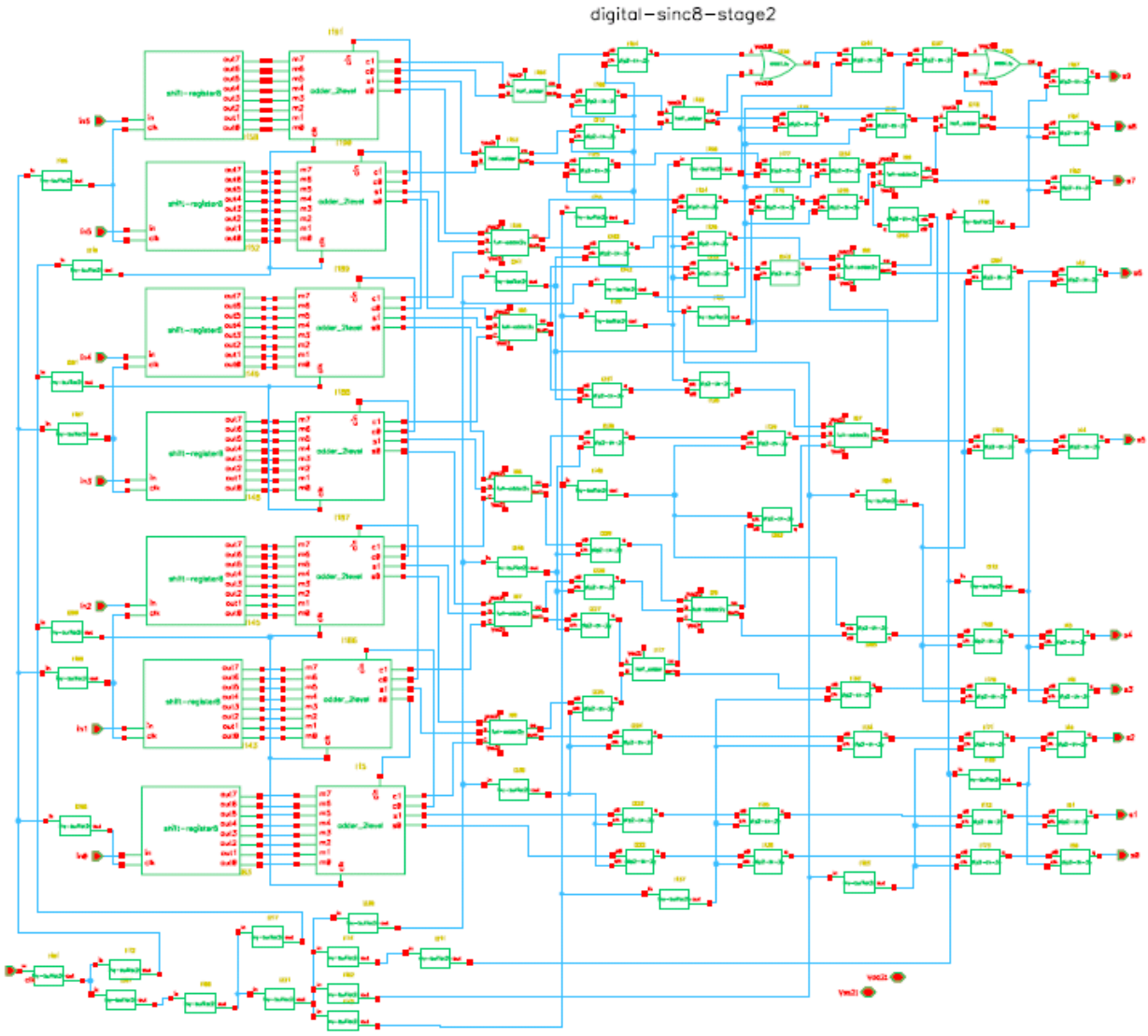

Figure 2.49 Second Stage Digital Filter Top Level Schematic Circuit

Third stage and fourth stage filters are essentially implemented in the same architectures as first one, so they will not be discussed.

Figure 2.46 is implemented with TSMC 0.18um technology and simulated through Cadence Virtuso Analog Design Environment tool. The time domain simulation results

are presented in Figure 2.50 and Figure 2.51 for a 50 MHz sine wave input and a 10 MHz sine wave input respectively. The amplitude for each case is 0.4 volts. It is observed that the weighted sum output of Figure 2.50 and Figure 2.51 are much closer to the analog input than the weighted sum output of the single first order delta sigma modulator as seen in Figure 2.33, which is concluded that the filter reduces the conversion error and increases the ADC resolution. This matches the theoretical discussion.

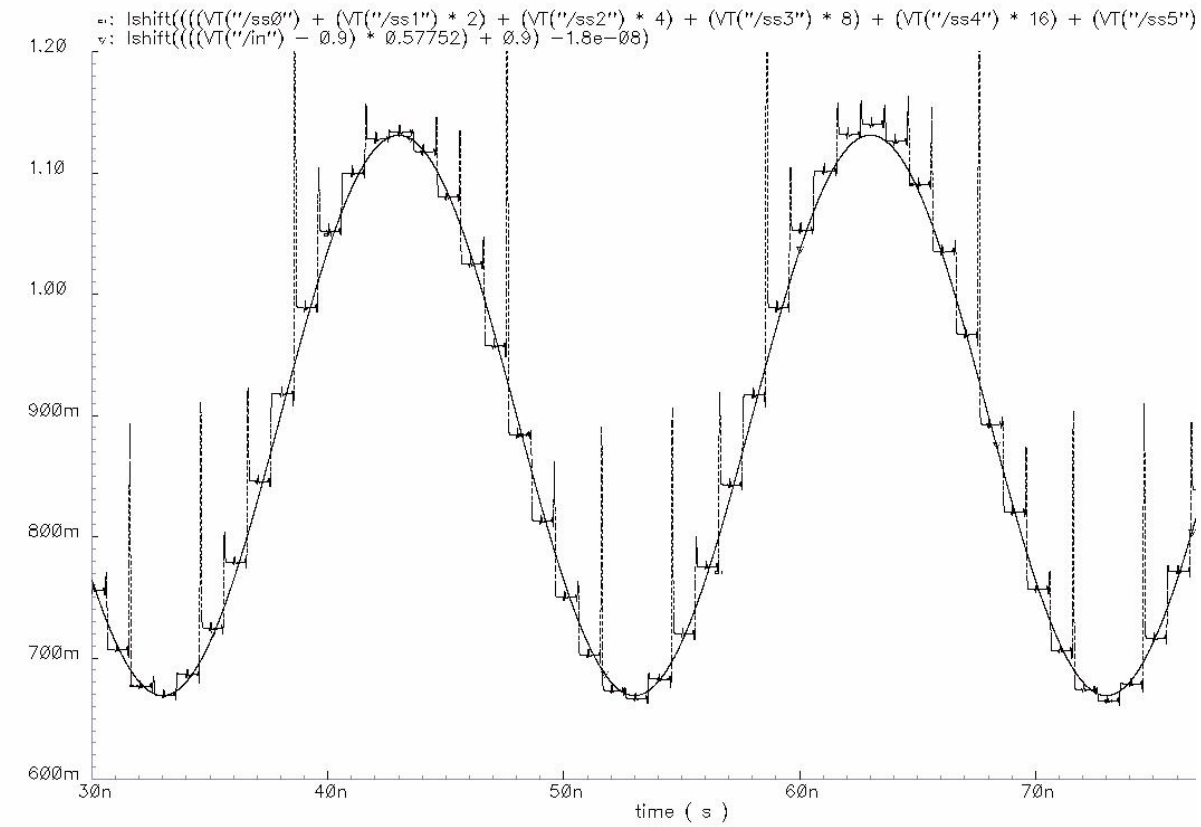

Figure 2.50 Schematic Simulation Results for Two Stage Digital Low Pass Filter with 50 MHz Input

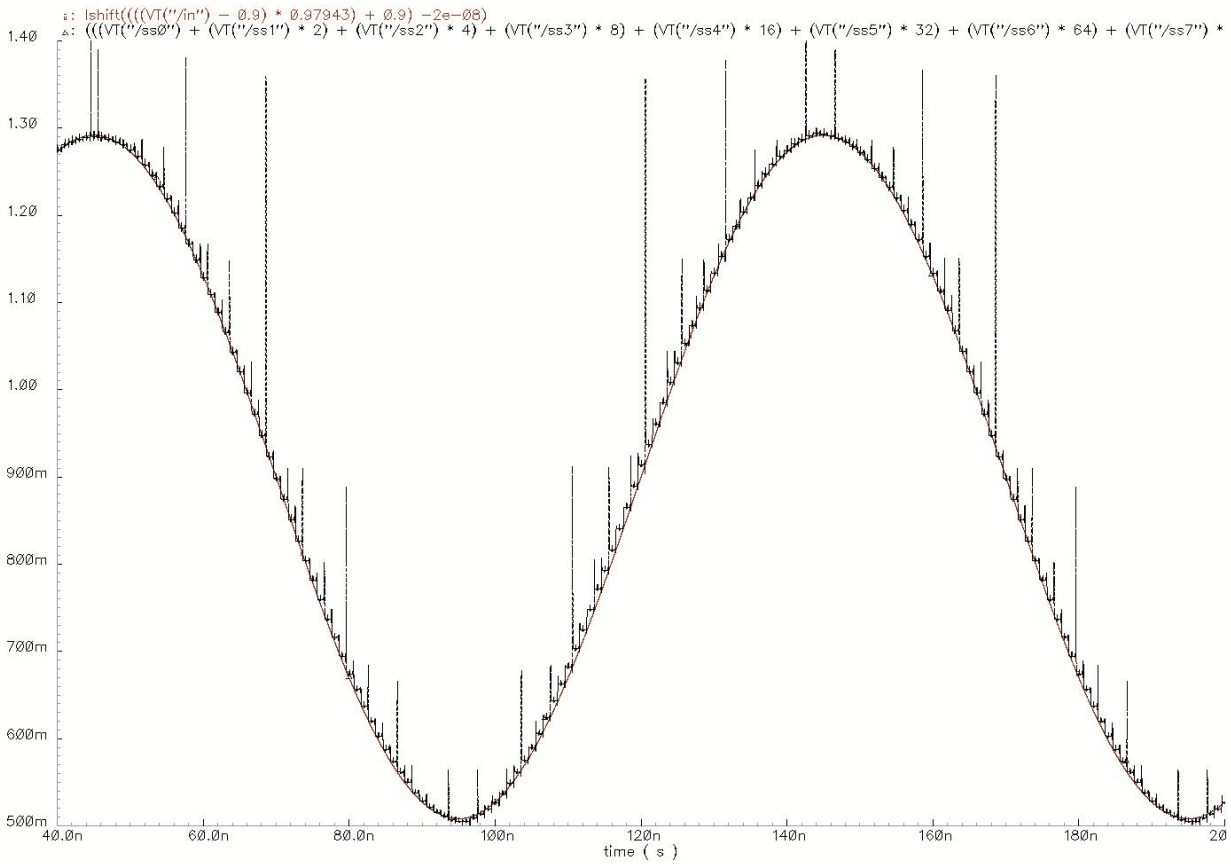

Figure 2.51 Schematic Simulation Results for Two Stage Digital Low Pass Filter with 10 MHz Input

The custom layout for the two stage digital filter is captured as shown in Figure 2.52 with total size of 661um by 491um which includes the power buses. As seen in Figure 2.52, the first stage digital filter is located in the left side of the layout and the second stage digital filter is arranged in the right side of the layout. The power buses are surrounding them.

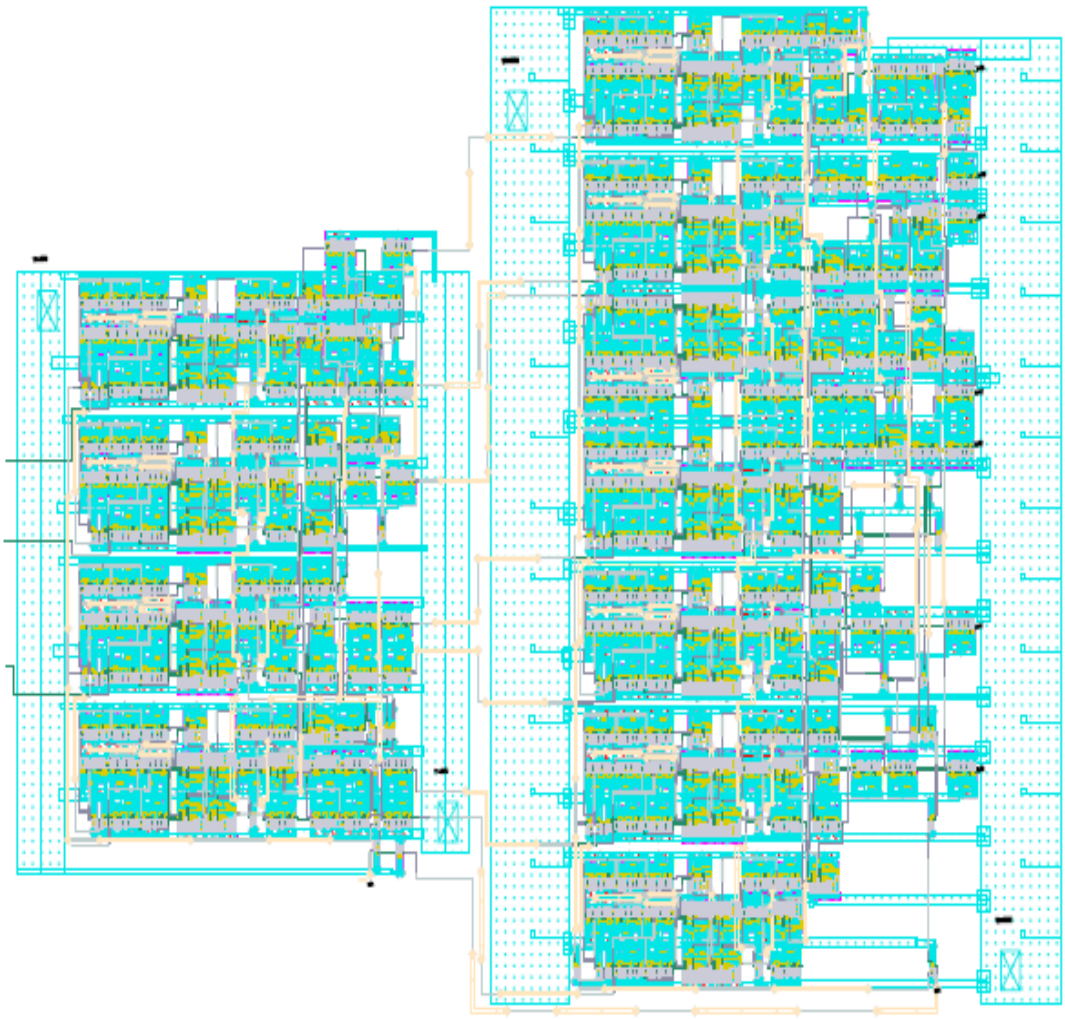

Figure 2.52 Two Stage Digital Filter Layout

Figure 2.53 shows the first stage digital filter layout extraction simulation results. The figure includes the ideal input signal to the first order delta sigma modulator ADC and the 10 bit weighted sum of the filter outputs. The inputs to the filter are the 4 bit digital output of the first order delta sigma modulator ADC whose results are shown in Figure 2.33. It can be seen that the output weighted sum of the first stage filter is much smoother than input weighted sum of the filter

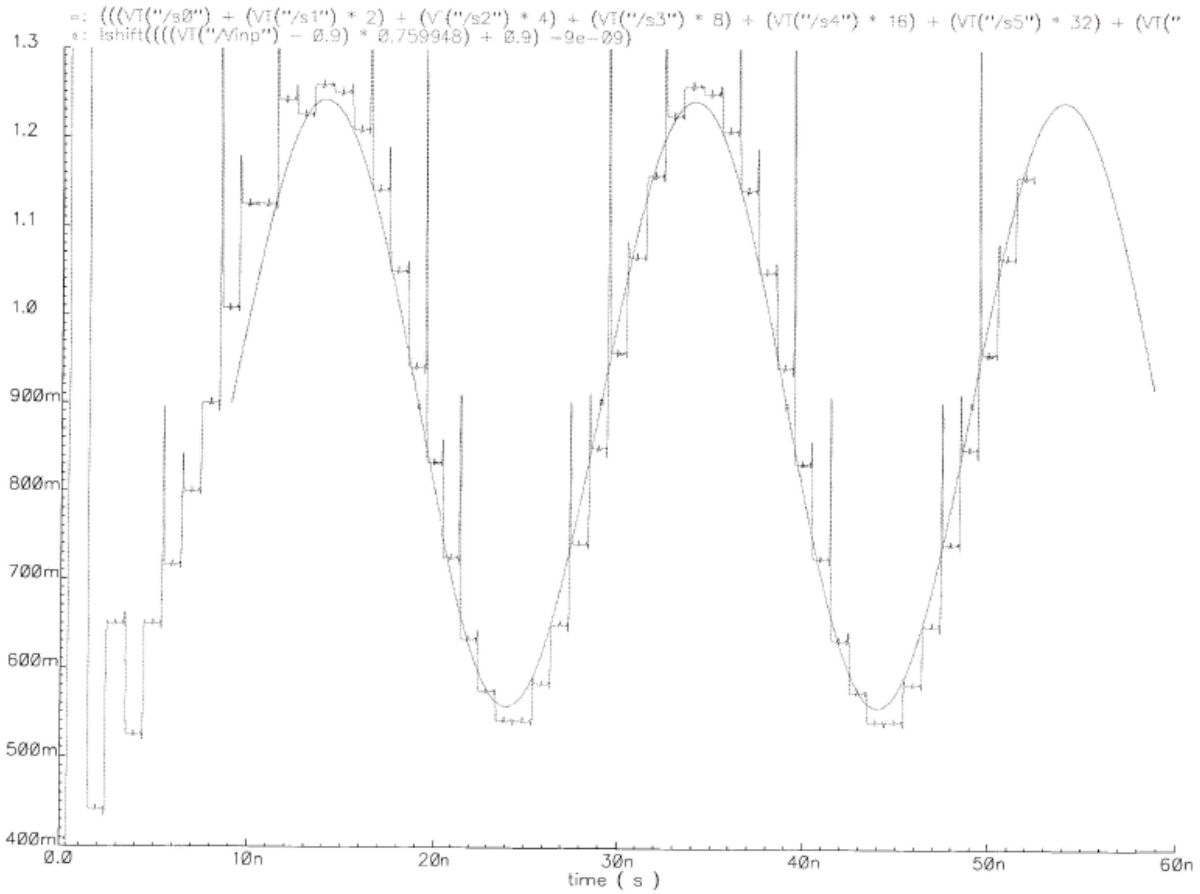

Figure 2.53 First Stage Digital Filter Layout Simulation Results

Figure 2.54 gives the second stage digital filter layout extraction simulation results. Again, the figure includes the ideal input signal to the first order delta sigma modulator ADC and the 13 bit weighted sum of the filter outputs. The inputs to the filter are the 7 bit digital output of the first digital filter as seen in Figure 2.47. It can be seen that the second stage filter output weighted sum is more matching to the ideal input than the first stage filter weighted sum.

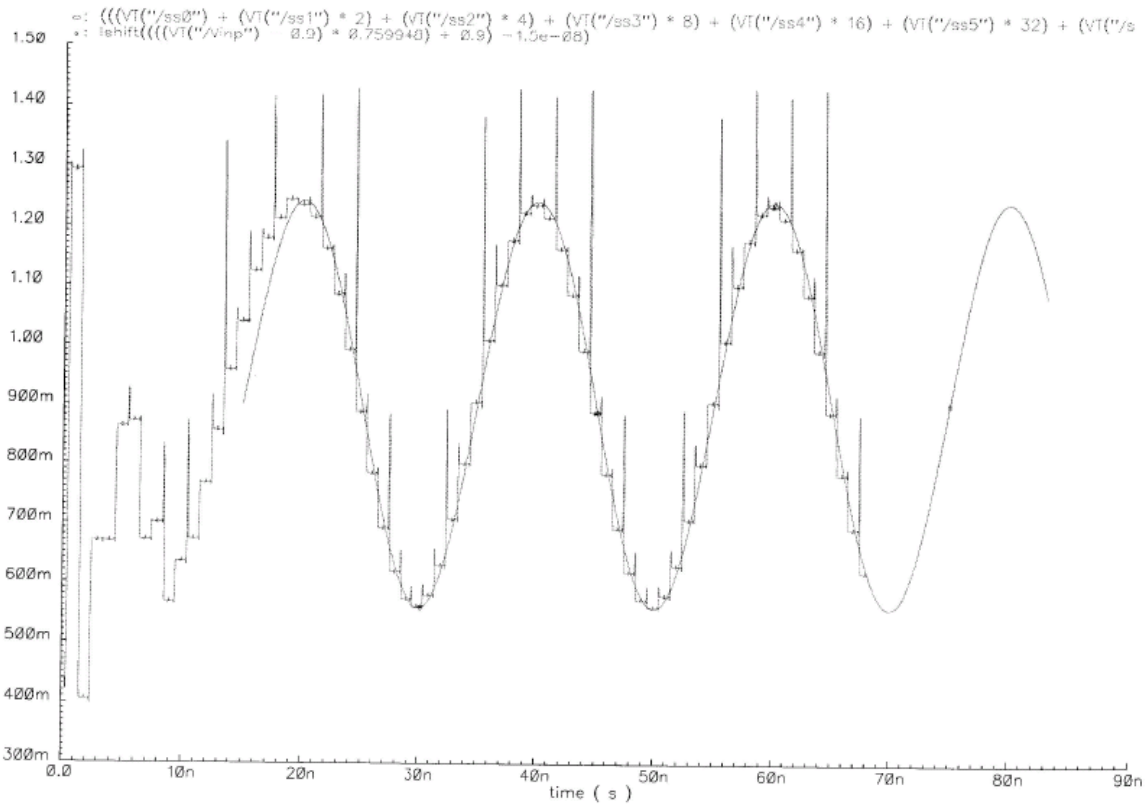

Figure 2.54 Two Stage Digital Filter Layout Simulation Results

2.5 Two Stage PDSM ADC Cadence Simulation Result

The 0.18 um CMOS schematic version of the entire PDSM ADC was simulated using the Cadence Analog Design Environment. The output data was captured. The weighted sums of the digital output of each stage are combined analytically with the proper shifting to produce an analog version of the final output. The results for a 50 MHz input are as shown in Figure 2.55 and for a 10 MHz input are shown in Figure 2.56. It can be seen the weighted sum is matching the analog input very well from time domain. The input is a sine wave with amplitude of 0.2 volts and a frequency of 50 MHz and 10MHz respectively. The clock with frequency of 1 GHz is distributed throughout the PDSM ADC using a standard tree structure with buffers, so the simulation results include the effect of clock jitter.

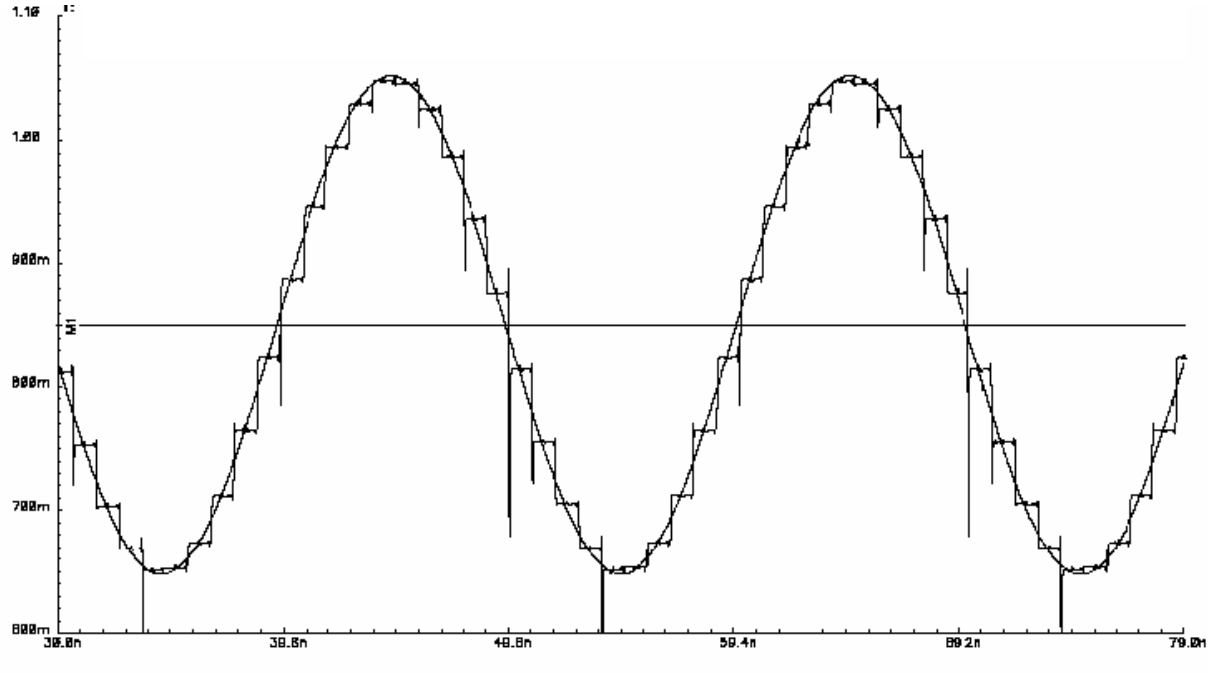

Figure 2.55 Two Stages PDSM ADC Schematic Simulation Results of 0.18um CMOS Design for 50 MHz Input

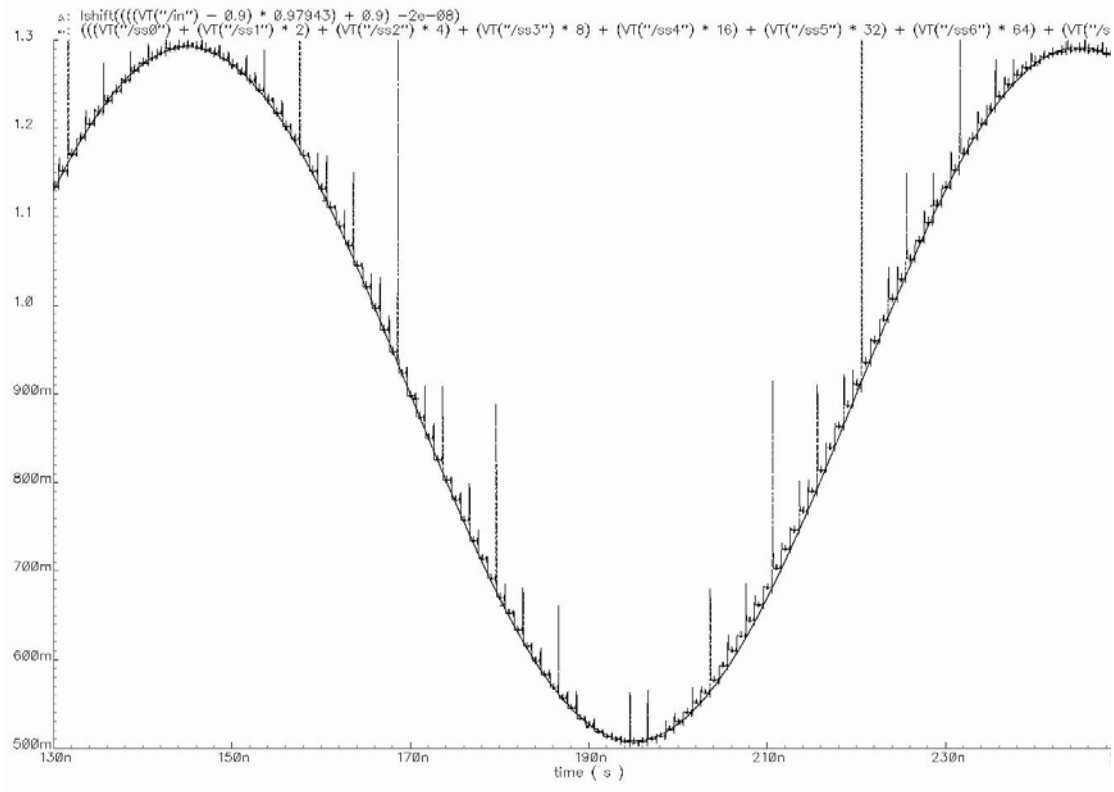

Figure 2.56 Two Stages PDSM ADC Schematic Simulation Results of 0.18um CMOS Design for 10 MHz Input

Figure 2.57 shows the FFT of the weighted sum of output of the first stage after low pass filtering and Figure 2.58 shows the FFT of the final output after combining the weighted sums of the first and second stage outputs.

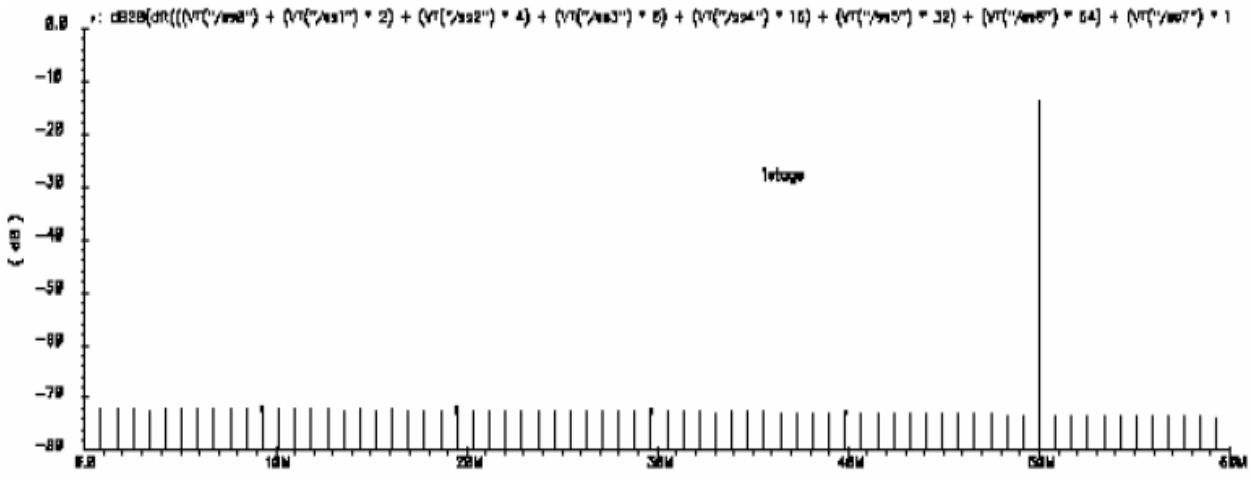

Figure 2.57 First Stage PDSM ADC FFT Results for 0.18um CMOS Schematic Design

Note: the x-axis scales on Figure 2.57 are 0.0, 10M, 20M, 30M, 40M and 60M
The y-axis scales are -80, -70, -60, -50, -40, -30, -20, -10, 0.0 in unit of db

Based on the data presented for the FFT of stage 1 as shown in Figure 2.57, the signal to noise ratio over the 50 MHz bandwidth is calculated and found to be 40.91 db. This corresponds to an effective number of bits (ENOB) from the first stage of 6.5 bits. This result is consistent with the design objective of 6-7 bits from the first stage without the compensation filter. From the data presented for the FFT after combining the first stage and second stage outputs of the two stage PDSM ADC as shown in Figure 2.58, signal to noise ratio for a 50 MHz bandwidth was calculated and found to be about 76 db. This corresponds to about 12 bits of resolution. The SFDR is 81.79 db. The resolution of the FFT is constrained by the time length of the simulation, which is 1.2 u-seconds.

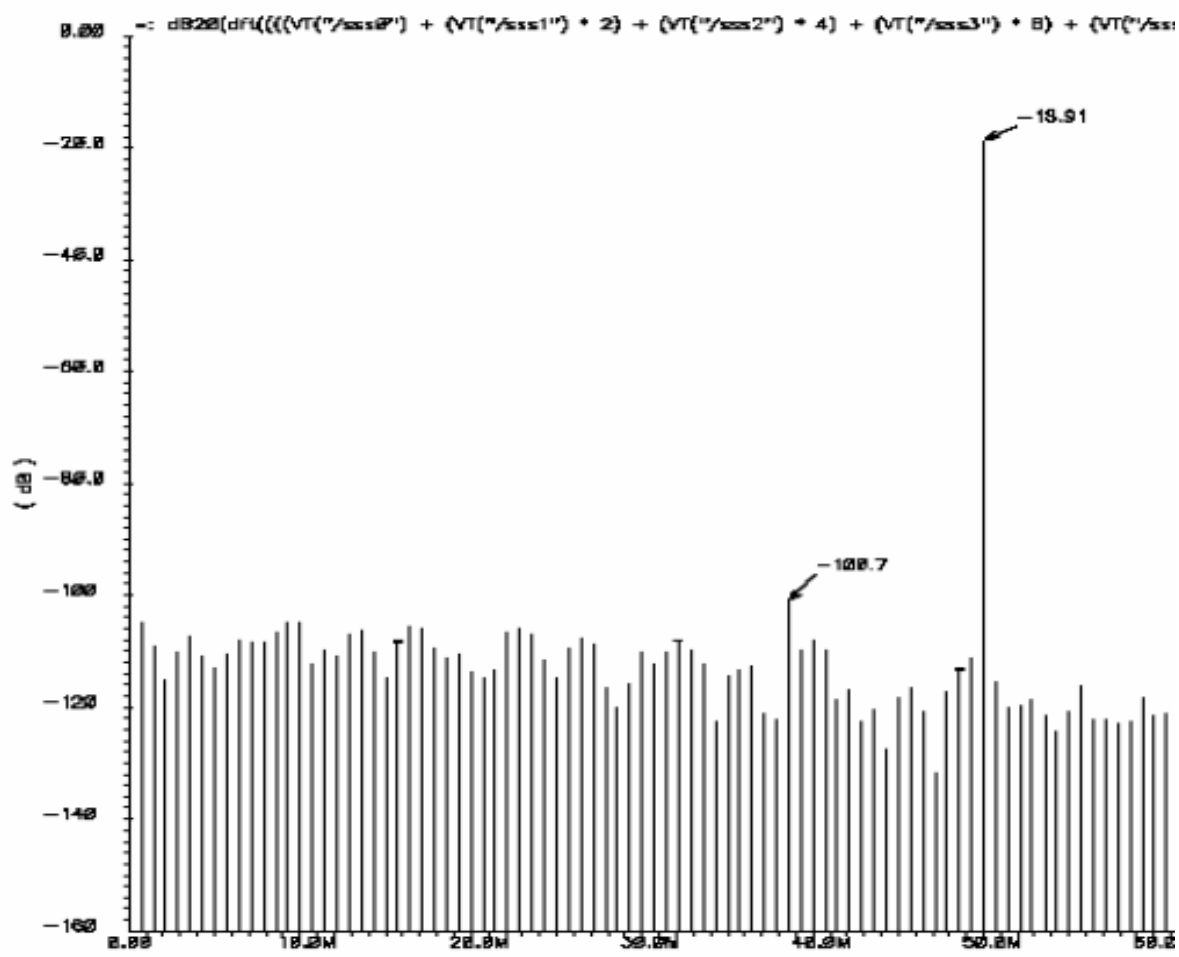

Figure 2.58 Two Stages PDSM ADC FFT Results for 0.18um CMOS Schematic Design

Note: the x-axis scales on Figure 2.58 are 0.0, 10M, 20M, 30M, 40M and 60M
The y-axis scales are -80, -70, -60, -50, -40, -30, -20, -10, 0.0 in unit of db

Table 2.2 compares some key performance parameters of the Pipelined Delta Sigma Modulator (PDSM) ADC using the residue averaging technique with some state-of-the-art pipelined ADC designs. The PDSM ADC has a wide bandwidth (62.5 MHz) combined with high resolution due to the benefits of the over sampling, delta sigma noise shaping, and residue averaging. The high sampling frequency (1 GHz) of the PDSM

ADC results in a relative large power consumption (950 mW) compared to the other designs.

Table 2.2 Performance Summary of PDSM ADC and State of the Art Pipeline ADCs

Design	This Design	[76]	[77]	[78]	[79]	[80]	[81]
Technology (CMOS)	0.18μm	0.18μm	0.35μm	90nm	0.18μm	0.25μm	0.18μm
Supply Voltage	1.8v	1v	3v	1v	2.8v	1.3v	1.8v
Technique	ΔΣ modulator with averaging technique	Switched-opamp using loading free architecture	Flash ADC with incomplete settling	Capacitance coupling techniques	Digital distortion calibration	SC with bootstrapped switches	SC
Sampling Rate	1GS/S	100MS/S	75MS/S	100MS/S	20MS/S	16.384MS/S	110MS/S
Input frequency	62.5MHz	1.5MHZ	37.5MHZ	10MHZ	1MHZ	8.75MHZ	10MHz
Resolution	13b	8b	12b	10b	14b	13b	12b
SNDR	76db	41.5db	63.5db	55.3db	71.6db	59.2db	64.2db
SFDR	81.79	52.6db	71.2db	71.5db	82.3db	62.5db	72.8db
Power Consumption	950mW	30mW	308mW	33mW	34.8W	78mW	97mW

2.6 Prototype Tape Out

Two prototypes have been taped out. The block diagram of the first prototype is shown in Figure 2.59, which integrates one stage PDSM with the on chip clock generator. The final layout is shown in Figure 2.60 which was realized in a 7 mm^2 die, the minimum size of MOSIS offered for TSMC 0.18um process.

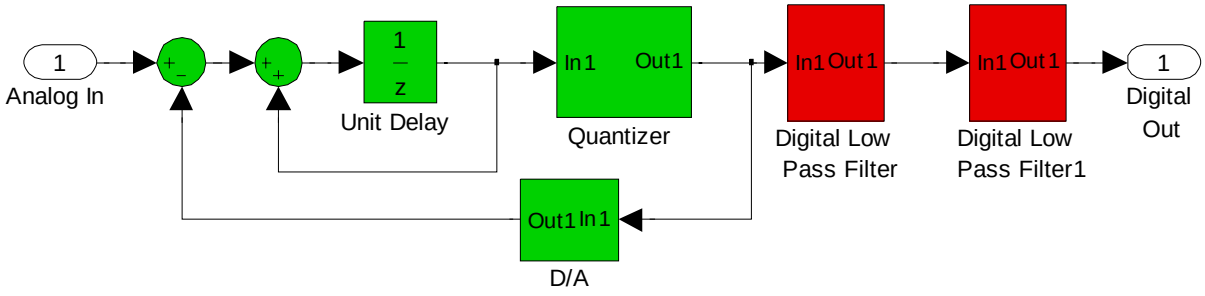

Figure 2.59 First Prototype Block Diagram

From Figure 2.60, it can be seen that there are 40 pads on the square frame with 10 pads on each side to accommodate the required inputs, outputs, biases, and internal, pad ring Vdd and Gnd inputs. The right side 13 pads of this layout are all related with the on chip digital components. The 13 pads include 8 bits digital outputs, one pair of pad ring power supply, one pair of on chip digital power supply and one external clock source input. The left side 37 pads of this layout are all have connections with the on chip analog components. It can be seen the analog and digital pad rings are separated on both top and bottom right. This is the way to eliminate the digital effect on the on chip analog circuits and to reduce the noise level and improve the ADC performance.

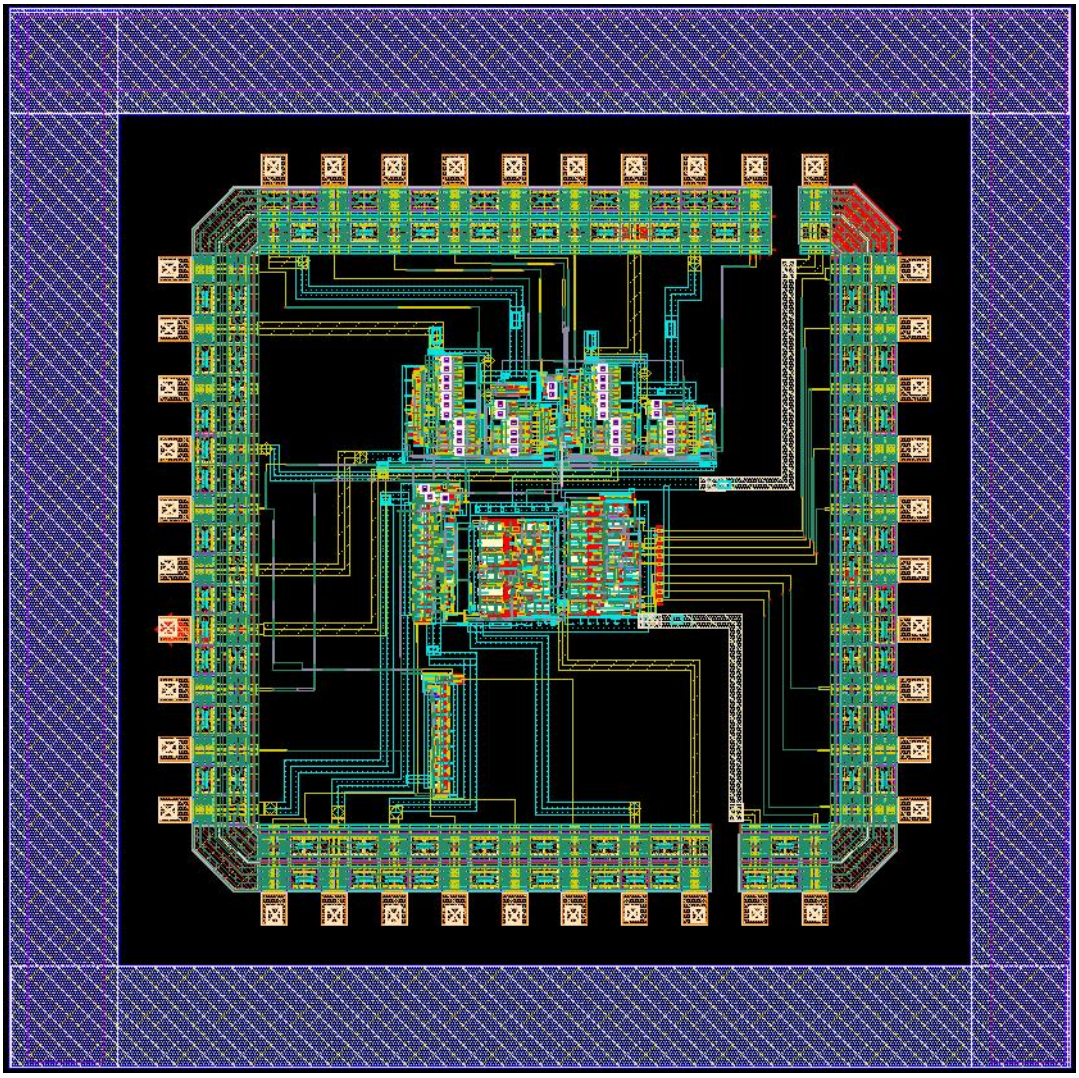

Figure 2.60 First Prototype of One Stage PDSM

The second prototype is a two stage PDSM ADC. The layout is shown in Figure 2.61 which does not include the density fill.

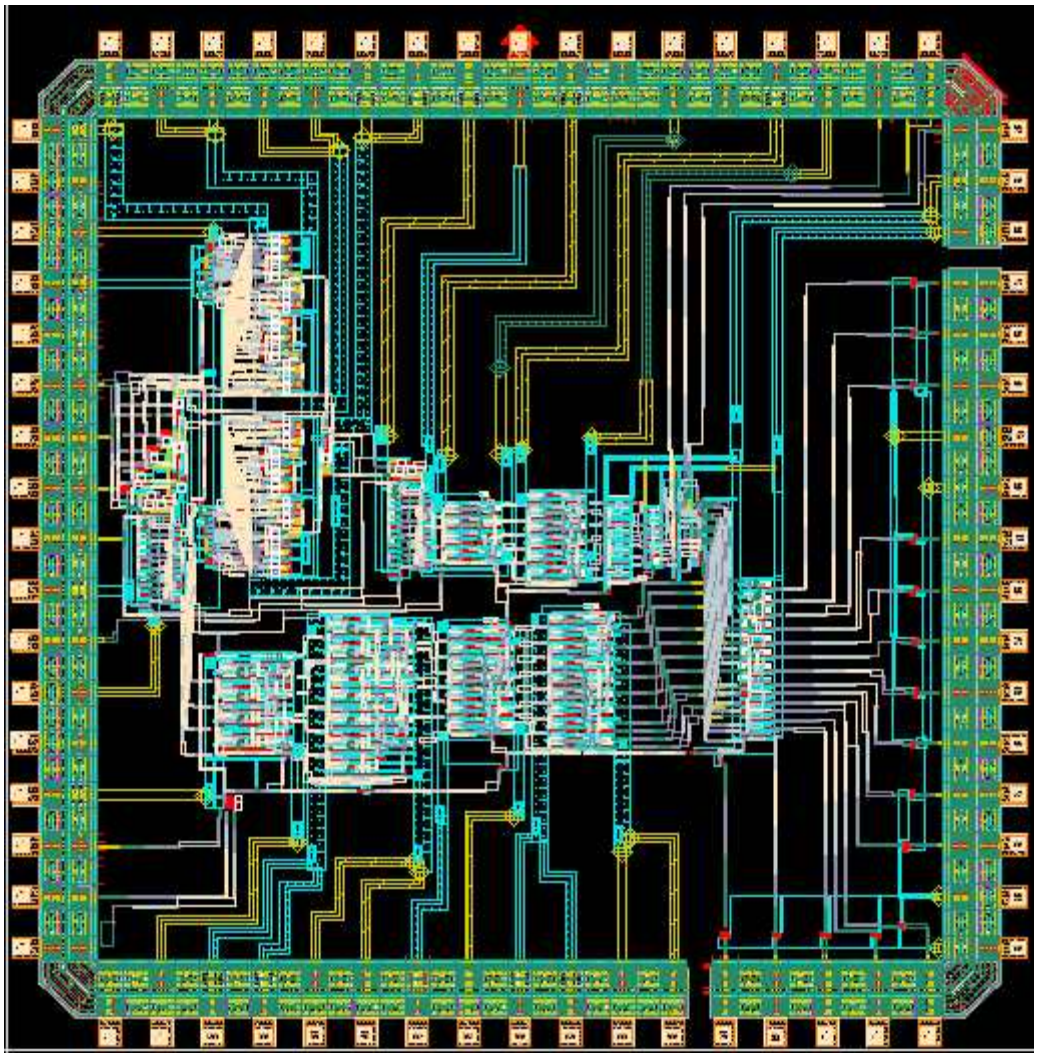

Figure 2.61 Layout of Two Stage Pipelined Delta Sigma ADC (No Fill)

As seen in Figure 2.61, there are 68 pads on the square frame with 17 pads on each side to accommodate the required inputs, outputs, biases, and internal and pad ring Vdd and Gnd inputs. The outer dimension of the frame is 2975um by 2975um. The layout including the fill layers is shown in Figure 2.62. The fill layers are required for metals 1-6, capacitor, and poly to meet the minimum density requirement for each of the layers. In this case some fill was added to the perimeter of the top and left hand side of the frame as well as to the internal of the frame. This was done carefully, so not to cause any problem

to the chip, such as short circuit, even additional parasitics. The overall dimension of the chip with fill is 3162umx3162um. This is just under the new minimum chip size for the TSMC 0.18um process which is 10 millimeters square.

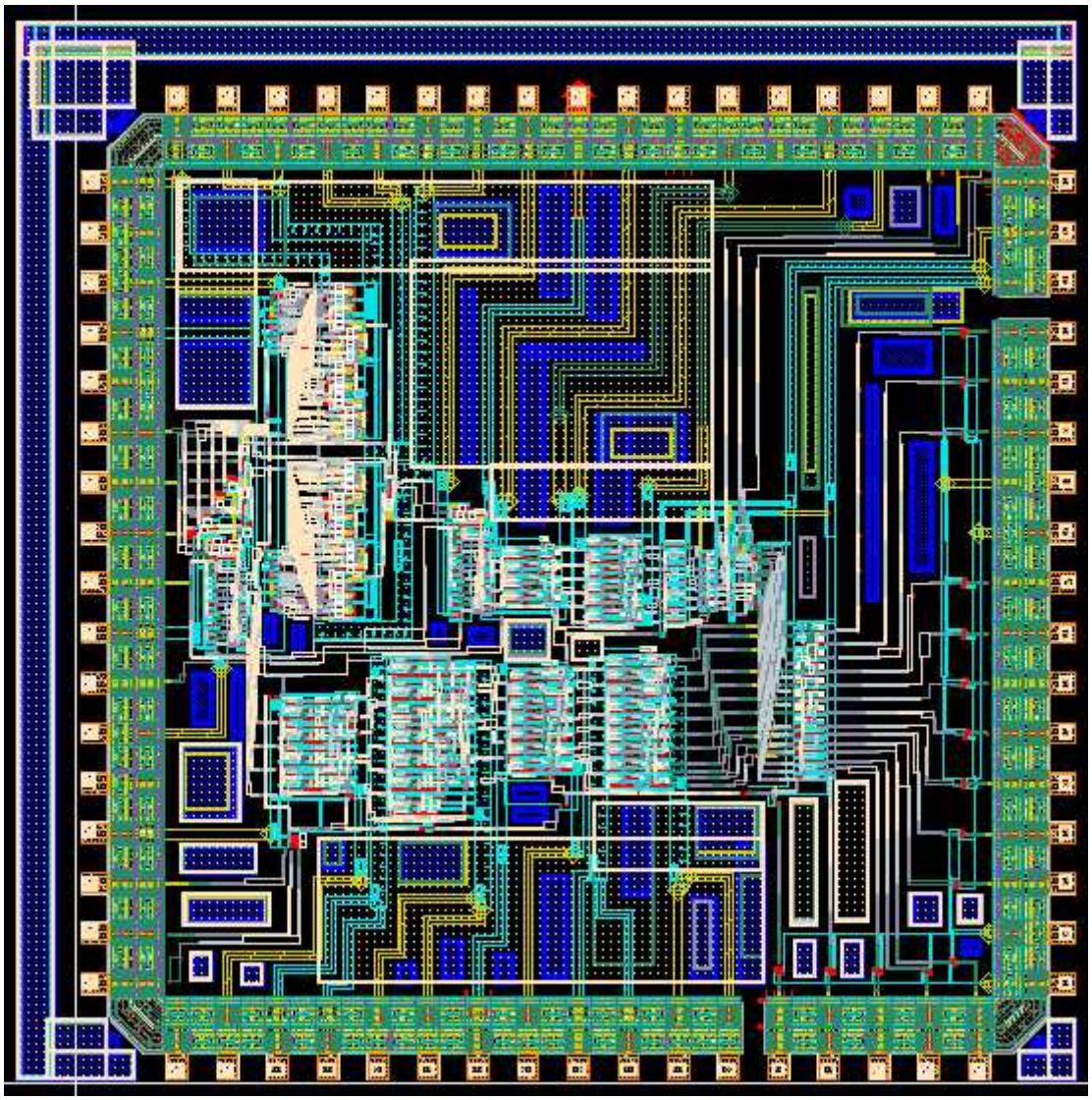

Figure 2.62 Layout of Pipelined Delta Sigma ADC (With Fill)

The functionality of the layout was verified by running simulations based on inputs and outputs at the pad level after extracting a net list from the layout. Figure 2.63 illustrates the weighted sum of the outputs for stage 1, stage 2, and the final output for a 50 MHz

sine wave input at 1.0 GHz sample frequency. As shown in Figure 2.63, the top figure is the weighted sum of the second stage digital outputs; the middle one is the weighted sum of the first stage digital outputs; the last one is the combination of the two stages with proper correction function.

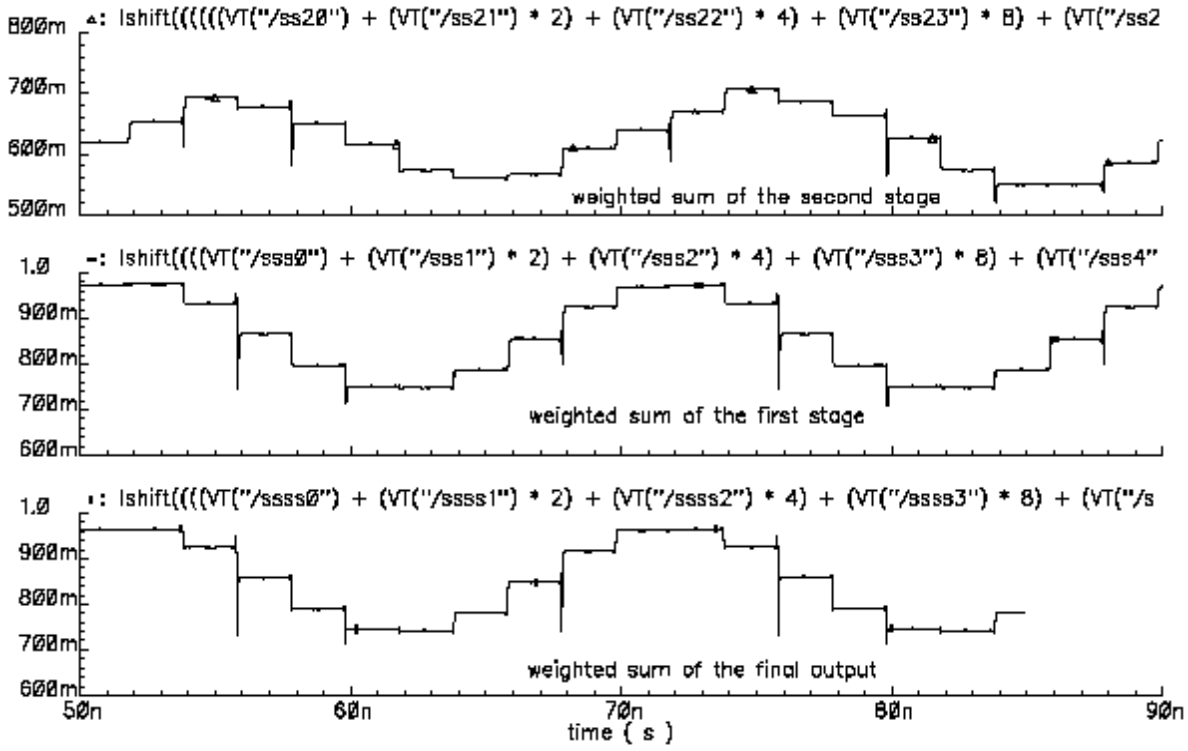

Figure 2.63 Two Stage PDSM ADC Simulation Results Based on Layout Net List With 50 MHz Input and 1 GHz Sample Frequency

Top figure: weighted sum of the second stage digital outputs
Middle figure: weighted sum of the first stage digital outputs
Bottom figure: combination of stage one and stage two outputs with proper correction.

2.7 First Prototype Measurement Results

The layout of the one stage PDSADC shown in Figure 2.60 was initially packaged in a 40 pin DIP package and its test fixture is shown in Figure 2.64. Because the 40 pin DIP package and socket have significant parasitic capacitance and inductance associated with

the pin outs and package, the testing results are not promising. So an alternative custom quad-flat package was designed and fabricated and the test fixture is shown in Figure 2.65. The custom Quad-Flat Package is not inserted into any socket for this PCB, but rather has the package leads soldered directly to the board wires. Also the die I/O pads are connected to the package leads with micro-strip lines which avoid the use of bonding wire.

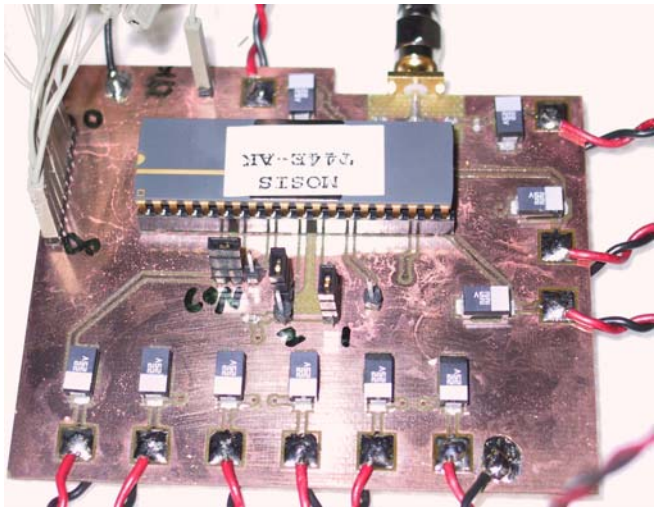

Figure 2.64 Test Fixture of DIP Package ADC

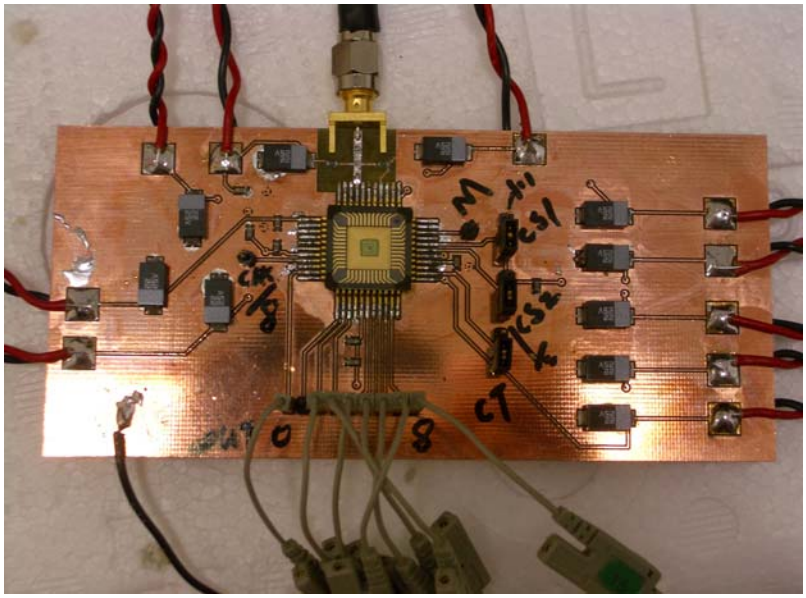

Figure 2.65 Test Fixture of Flat-Quad Package ADC

The following summarize some of the test fixture measurement results for the two test configurations as well as a comparison of the results.

Both PCBs include the following features to reduce the environment interference.

- Each DC input has a 0.1uF and a 22uF SMT capacitors to ground to mitigate both high frequency and low frequency noise effects. Each DC input has a separate twisted pair that is soldered to the PCB board to reduce the electron-magnetism effect.
- The analog input has a separate ground plane that is connected to the main ground plane at a single point to minimize analog signals interference.
- The DC offset for the analog input is accomplished with a voltage divider formed by two SMT resistors. The analog input is coupled to the SMA connector via a blocking capacitor to protect the input source to the chip.

The test environment using the PCB test fixtures is shown in Figure 2.66. The digital outputs of the ADC are captured using an Agilent 1683 AD Logic Analyzer.

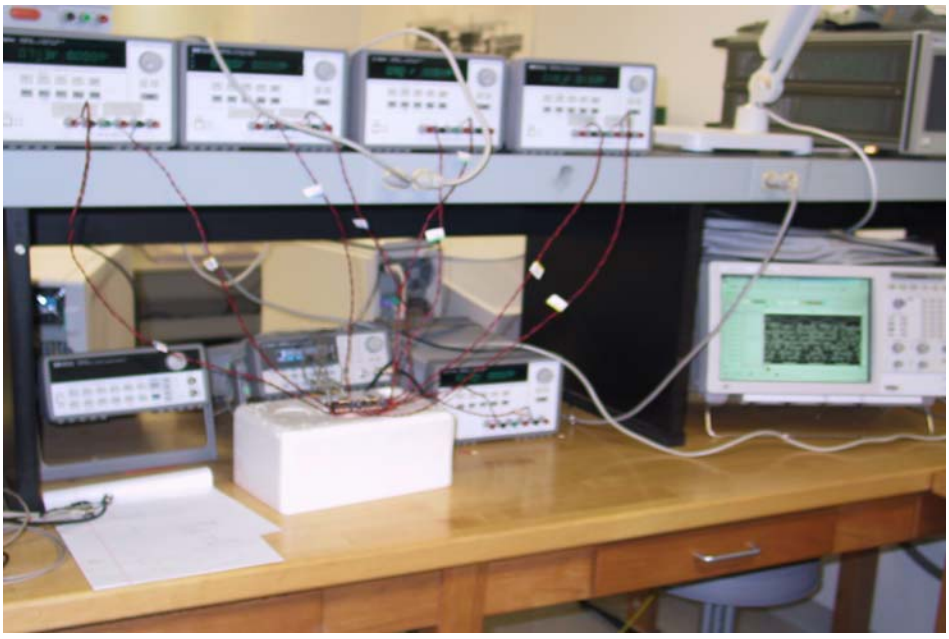

Figure 2.66 PDSM ADC Test Environment

For comparison purposes, the following results are presented for a single on chip clock frequency of 824 MHz. Since the maximum synchronous clock frequency of Agilent 1683 AD Logic Analyzer is 200 MHz, the ADC digital output data have to be decimated. The decimating factor is 8 which is built on the chip. With the decimation, the digital data are clocked off chip at 103 MHz rate.

Figure 2.67 and Figure 2.68 give the Agilent HP 1683 AD logic analyzer testing results for both PCB configurations for 1MHz input and 824 MHz on chip clock. As seen in Figure 2.67 and Figure 2.68, the top signal shows the measuring sample number; the second top signal is the weighted sum of the digital outputs displayed as an analog signal and the following 8 signals are 8 bit digital signals of the ADC from top LSB to bottom MSB; the bottom signal gives the measuring time range. It can be observed that the MSB (My Bus 2[7] as seen in the measurement figures) is a square wave pulse having the period of the input signal and the LSB (My Bus 2[0] as seen in the measurement figures) updates the data maximally in the decimated clock signal period. Both Figure 2.67 and Figure 2.68 show the two PCBs are working well functionally with 1MHz weighted sum of digital output matching the 1MHz analog input. The detailed resolution of the ADC has to be done by the FFT, so the time domain testing results will no longer be given after Figure 2.67 and Figure 2.68.

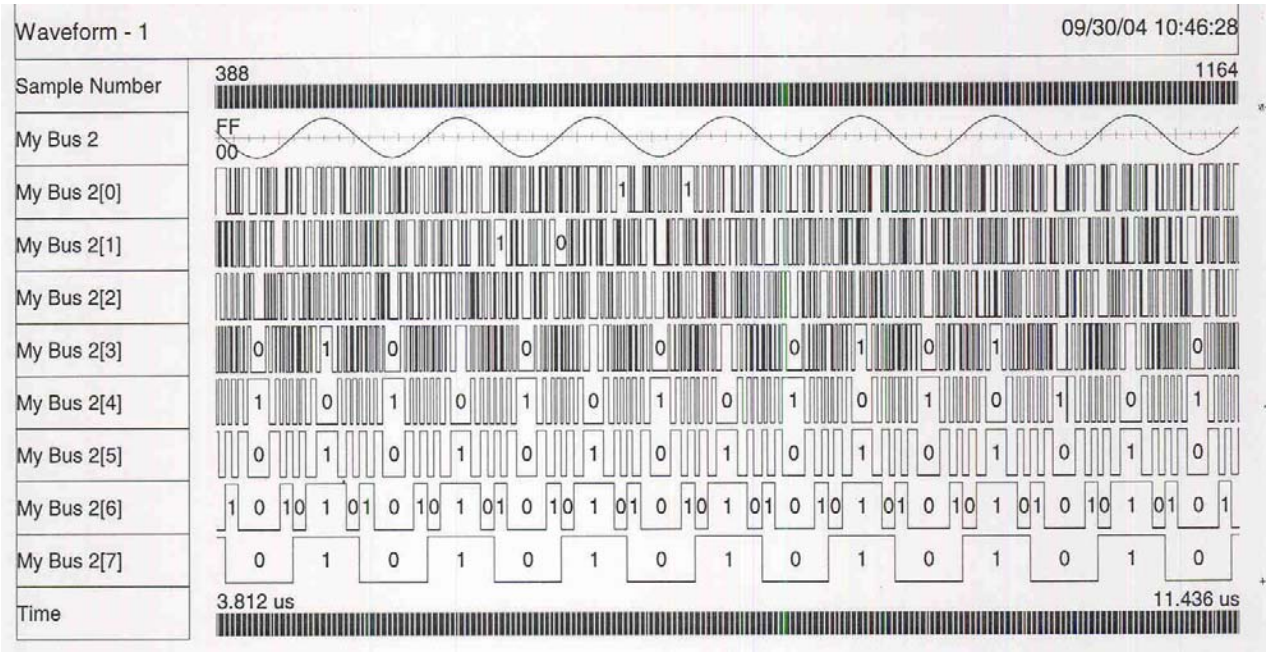

Figure 2.67 Test Results for On Chip Clock of 824 MHz Input 1 MHz

DIP Package PCB

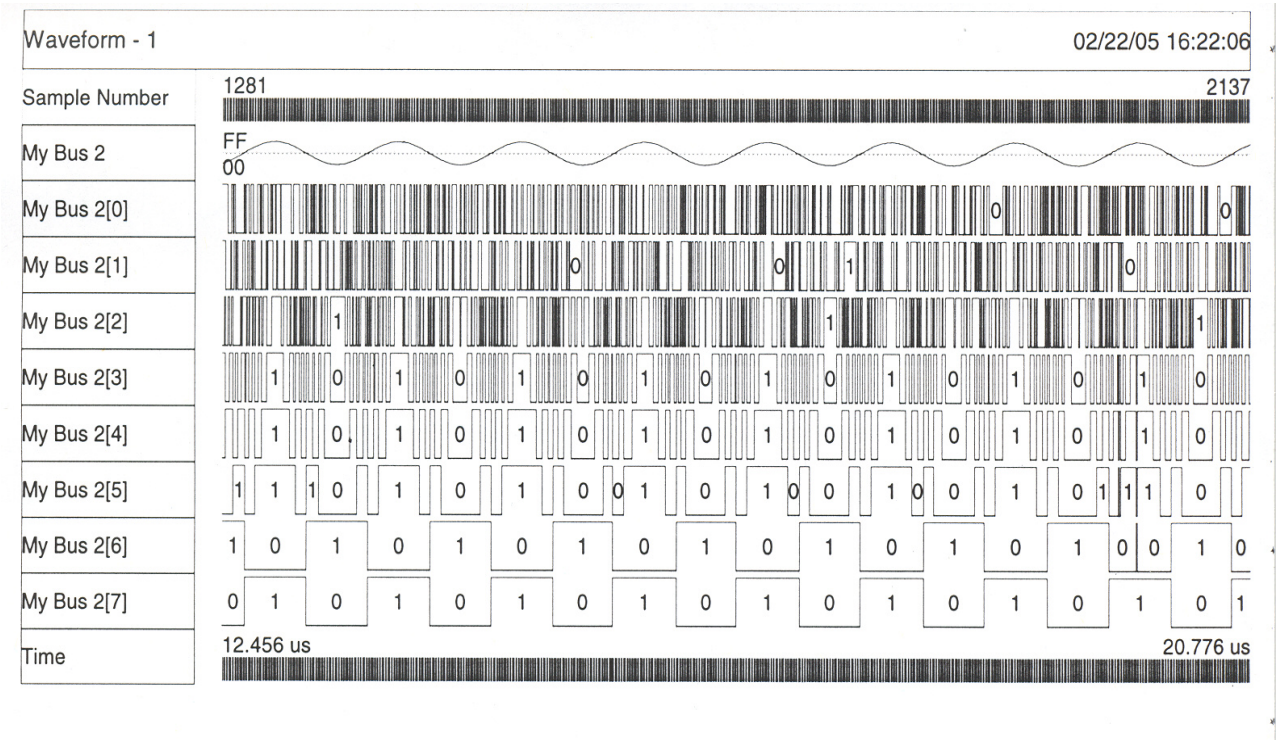

Figure 2.68 Test Results for On Chip Clock of 824 MHz Input 1 MHz

Quad-Flat Package PCB

The FFT results of the weighted sum of the digital outputs for several analog input frequencies are shown in Figure 2.69, Figure 2.70, Figure 2.71 and Figure 2.72, Figure 2.73 and Figure 2.74.

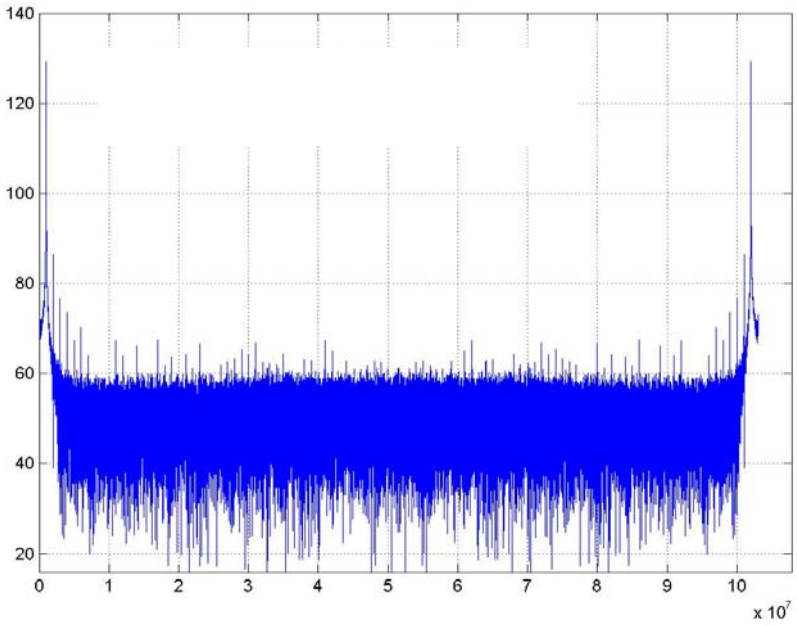

Figure 2.69 FFT Results for the 1 MHz Input On Chip Clock 824 MHz DIP Package PCB SFDR=45.26 db

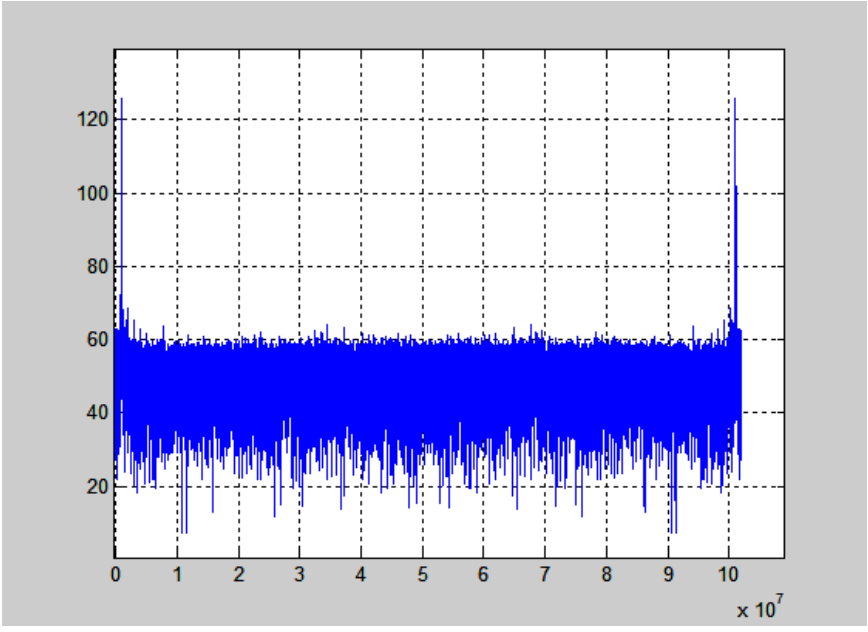

Figure 2.70 FFT Results for the 1 MHz Input On Chip Clock 824 MHz Quad-Flat Package PCB SFDR=61.56 db

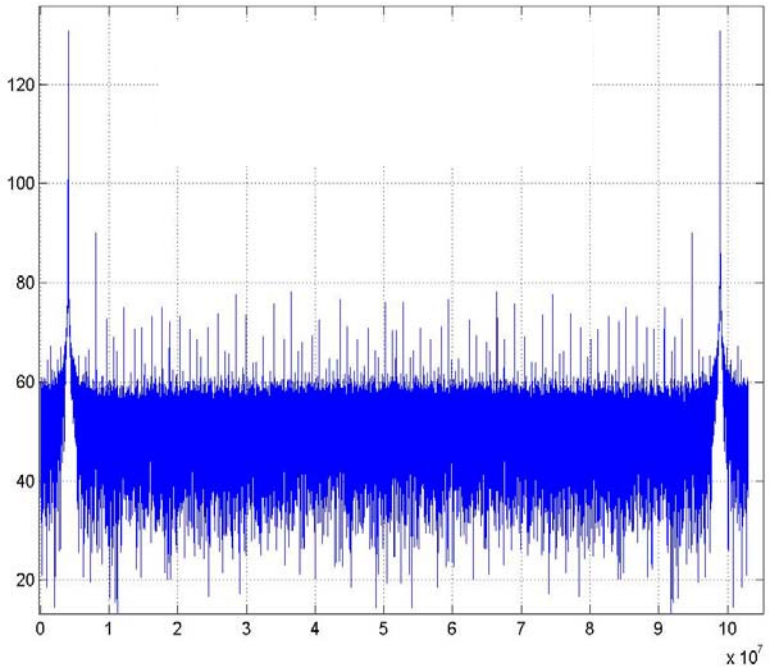

Figure 2.71 FFT Results for the 4 MHz Input On Chip Clock 824 MHz DIP Package PCB SFDR=43.21 db

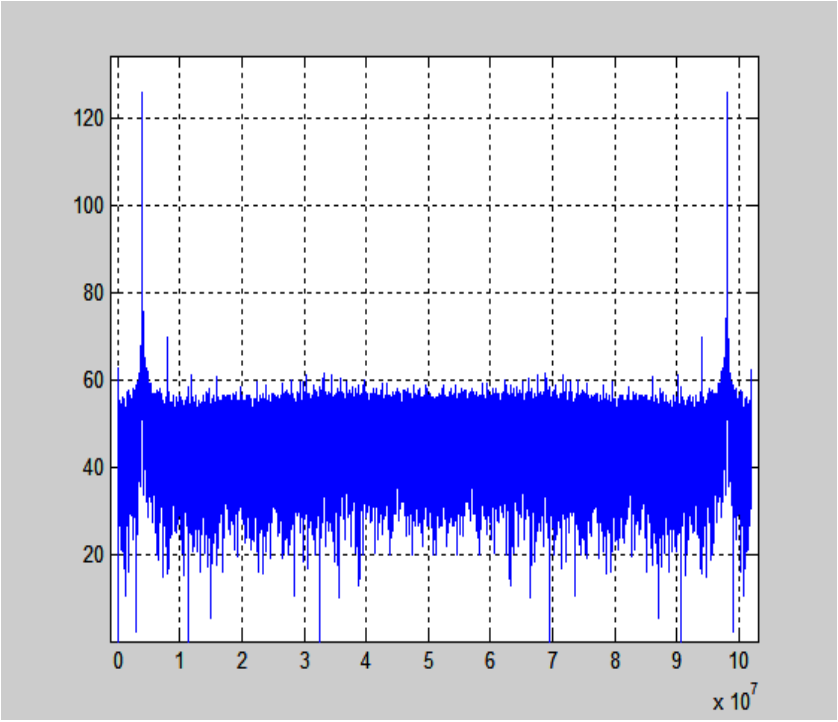

Figure 2.72 FFT results for the 4 MHz input On Chip Clock 824 MHz Quad-Flat Package PCB SFDR=61.56 db

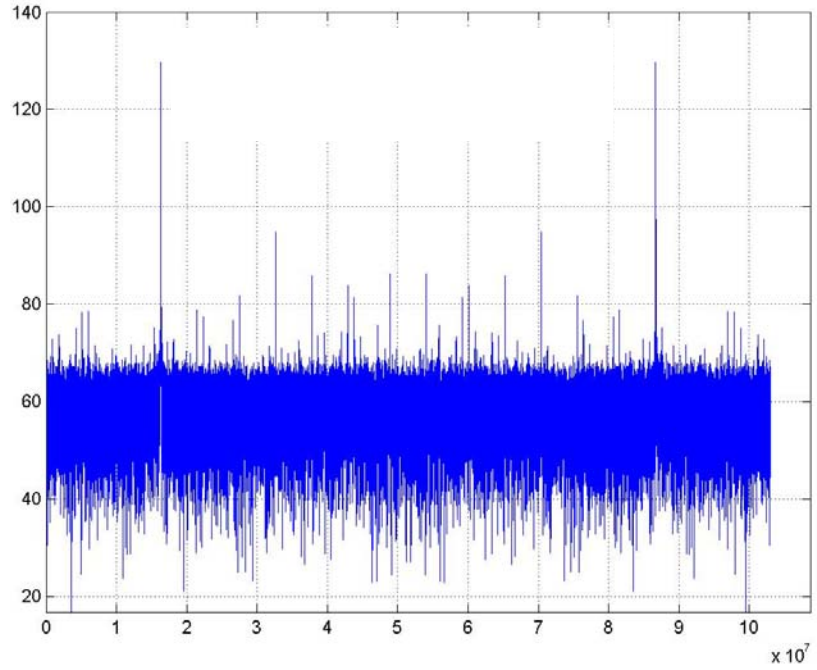

Figure 2.73 FFT Results for the 16 MHz Input On Chip Clock 824 MHz DIP Package PCB SFDR=38.75 db

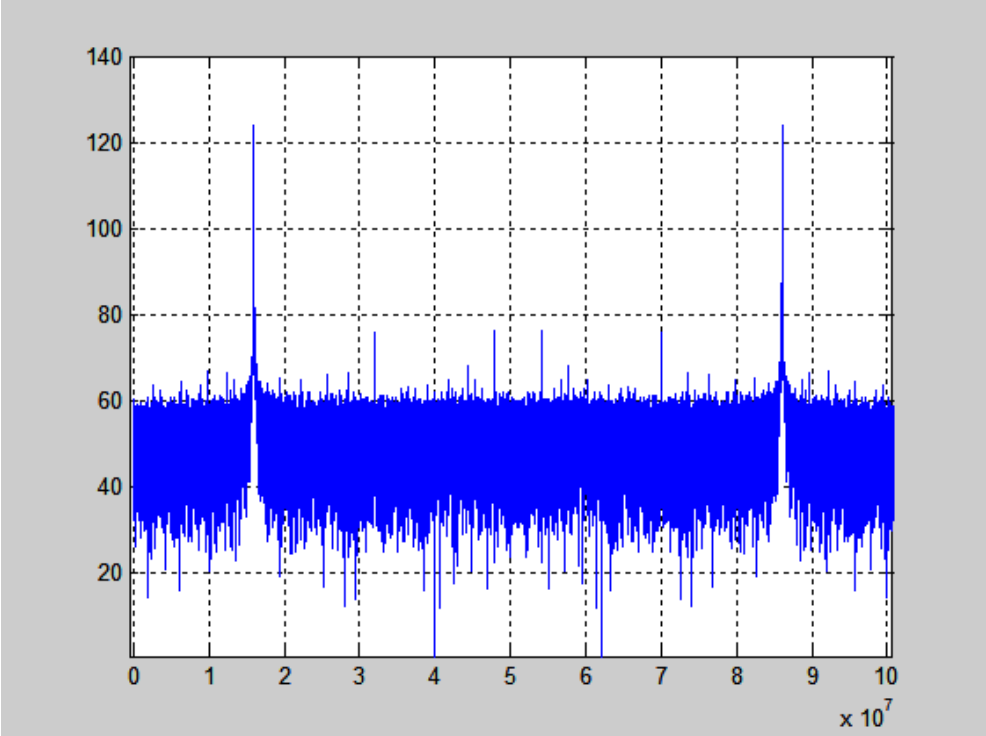

Figure 2.74 FFT Results for the 16 MHz Input On Chip Clock 824 MHz Quad-Flat Package PCB SFDR=47.73 db

The time domain data as presented in Figure 2.67 and Figure 2.68 look very similar for the two test configurations. However, comparing the FFT results we see that the noise has been reduced significantly in the custom Quad-Flat Package PCB test configuration. The Spur Free Dynamic Range (SFDR) for 1MHZ input is 61.56 db for the Quad-Flat Package PCB compared to 45.26 db for the DIP Package PCB as shown in Table 2.3. It is apparent from these results that the Quad-Flat Package with no socket results in a significant increase of the SFDR and a reduction in the number of harmonics and the noise floor. Figure 2.75 and Figure 2.76 show the most significant bit digital output as seen on an oscilloscope for the two test fixtures with 4MHz. Again it is seen the Quad-Flat Package has less noise modulating the digital output than the DIP Package.

From Table 2.3, it can be concluded that:

- First Stage of PDSM ADC functions at clock frequency of 824 GHz with resolution of 6-8 bits, which meets the design objective.
- Results of different test configurations confirm the importance of die packaging and PCB test board design, layout, and fabrication.

Table 2.3 Comparison of Quad-Flat Package PCB and DIP Package PCB

Input Frequency (MHZ)	Clock Frequency (MHz)	Quad-Flat Package PCB		DIP Package PCB	
		SFDR (db)	ENOB (bits)	SFDR (db)	ENOB (bits)
1	824	61.56	6.84	45.26	5.03
4	824	55.96	6.84	43.21	4.8
16	824	47.3	5.26	38.7	4.3

Figure 2.75 and Figure 2.76 show the ADC most significant bit digital output captured by the 100 MHz Oscilloscope for the two PCBs respectively. Comparing the two figures, it can be seen that the Quat-Flat package output signal is cleaner than the DIP package output signal, especially at the transition region.

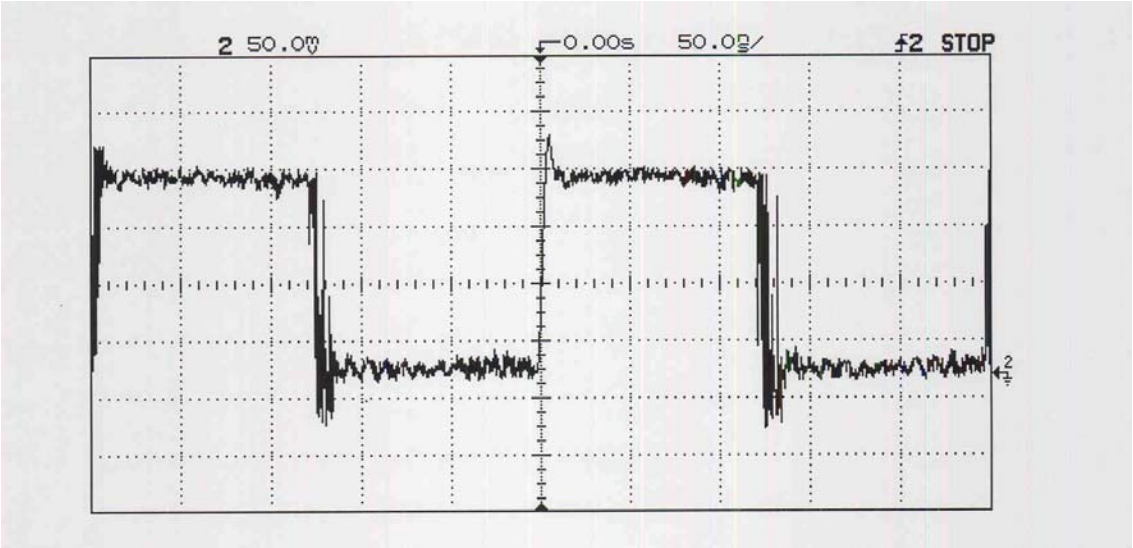

Figure 2.75 PDSM ADC Most Significant Bit Digital Output for On Chip Clock 824 MHz Input 4 MHz DIP Package

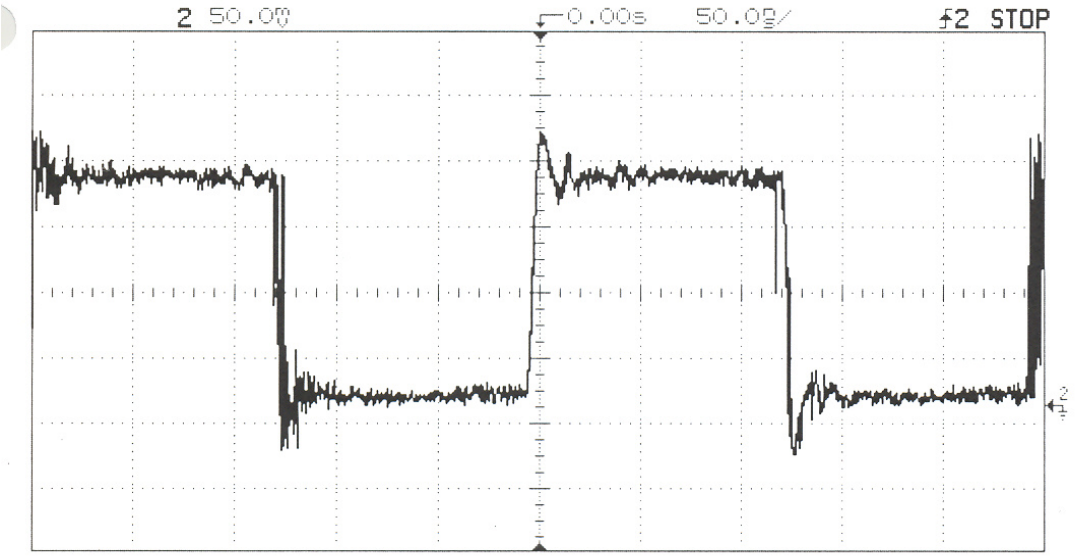

Figure 2.76 PDSM ADC Most Significant Bit Digital Output for On Chip Clock 824 MHz Input 4 MHz Quad-Flat Package

2.8 Conclusions

A unique architecture is presented for a high resolution, broad band ADC. The two stage PDSM ADC combines the features of over sampling delta sigma modulator ADCs with pipelined ADCs plus analog averaging technique. The result shows high resolution and broad band operation using first order modulators and relatively low over sampling ratios. The architecture has features which relax the requirements for component accuracy and matching which are well known of over sampling and delta sigma modulator features [82]. MATLAB simulation and FFT results were presented for the two stage PDSM ADC using sampling frequency of 1 GHz and an input bandwidth of 62.5 MHz. The MATLAB results support 13-15 bit resolution over the 62.5 MHz bandwidth. A transistor level 0.18um CMOS version of the design was captured using Cadence design tools with modulators and other components that can be clocked at 1 GHz. The FFT results, based on simulations of the CMOS 0.18um design, show 12 bit resolution with a 50 MHz input. These results support the practicality of using the PDSM ADC for applications where there is a need for high resolution and broad band operation. The prototype measurement for first stage PDSM ADC shows promising 6-8 bits with the proper die package and PCB set up.

3 Flexible RF/IF Band Pass Analog to Digital Converter for Multi-Channel Receivers

3.1 Introduction

Flexible multi-channel RF receivers for future wireless and sensor applications depend on moving the A/D interface closer to the antennae. A primary constraint in moving toward the "software radio" concept is the Analog to Digital converter [83,84]. Various RF front end architectures have been proposed to facilitate A/D conversion in the RF/IF region [85,86]. Some architectures have focused on band pass sub-sampling and signal processing prior to A to D conversion to relax the requirements on the ADC and to eliminate the need for the standard heterodyne mixer [87,88,89]. It is important that a sub-sampling receiver architecture support the generation of In phase (I) and Quadrature (Q) components for coherent receiver operation and image rejection. The I/Q components can be obtained prior to A/D conversion through the proper choice of sampling rates for the Sample/Hold sub-sampling mixer and with some added signal processing [87,88,90]. In this chapter a band pass ADC is presented, which is based on time interleaved (TI) first order delta sigma modulators (DSM). The unique TI DSM BPADC [91] is integrated with an RF receiver front end to achieve RF/IF A/D data conversion and I/Q down conversion with a simplified digital mixer.

This chapter will focus on the following efforts

- Investigate an architecture that supports flexible RF/IF center frequencies without changes in hardware.
- Center frequencies are modified by changing the clock frequency of the modulator, low pass filter and multiplexer.
- The resolution is determined by the modulator clock frequency and the bandwidth of the low pass (band pass) filters. The resulting bandwidth (fb) of the band pass ADC is twice that of the low pass filter centered at either fs or 3fs.

3.1.1 Receiver with Analog to Digital Conversion at Intermediate Frequencies

Flexible Multimode Receivers for future wireless applications depend on moving the A/D interface closer to the antennae. A receiver architecture with an IF Band Pass ADC and Digital I/Q (In-phase/Quadrature) mixer is defined as shown in Figure 3.1 below. The RF analog weak signal first passes through a tuned Low Noise Amplifier (LNA) to get a full scale RF signal. The band pass filter keeps the desired signal bandwidth with center frequency f_{RF} and eliminates the others. This filtered RF signal goes to a RF mixer which converts the signal to IF signal, that is $f_{If}=f_{RF}-f_{LO}$, where f_{LO} is the local oscillator frequency which is not shown on the figure. The IF signal out of the first stage mixer passes through an IF amplifier and then an IF band pass ADC. The digital signals out of the ADC are still in IF frequency, so a digital I/Q mixer is required to transfer the IF signals to base band frequency signals for the following digital processing. It is also important that the receiver maintain the ability to produce the I/Q components for purposes of image rejection and coherent demodulation. Building the CMOS IF ADC is a

challenging task. This chapter will focus on exploring some feasible IF ADC architectures.

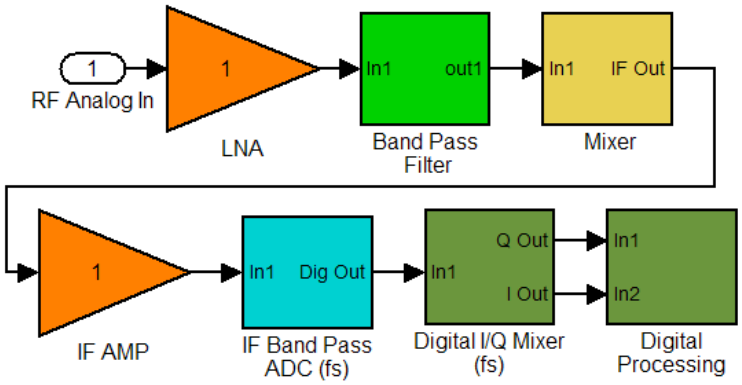

Figure 3.1 Receiver with IF Band Pass ADC and Digital I/Q Mixer

Figure 3.2 is a block diagram of the digital I/Q mixer that is clocked at the effective sampling rate of IF band pass ADC which will be discussed later.

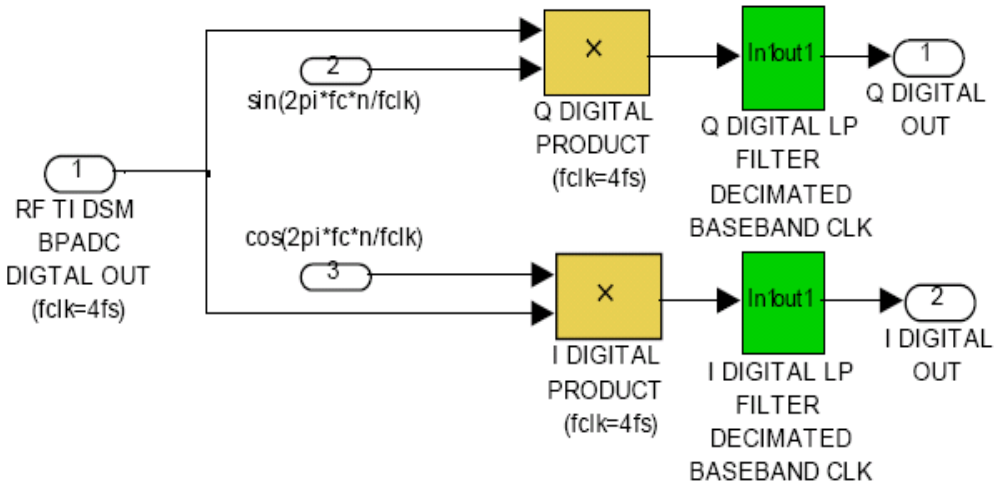

Figure 3.2 Digital I/Q Mixer

Forming the I/Q components in the digital domain avoids any analog mismatch problems. Note that generating the I/Q components is greatly simplified if $f_{if}=f_s/4$ or $3*(f_s/4)$. In this case $\cos(2\pi f_{if}*nT_s)=\cos(n\pi/2)=1, 0, -1, 0, \ldots$. Similarly, $\sin(2\pi f_{if}*nT_s)=\sin(n\pi/2)=0, 1,$

0, -1 …. In this special case, generating the I/Q components is simply an add/subtract operation (rather than multiply) in the digital domain. As will be discussed below, a time interleaved ADC with four or eight low pass ADCs facilitates the case where $f_{if}=f_s/4$ or $3*(f_s/4)$.

3.1.2 Multi-Channel Receiver Using IF Band Pass ADCs

A multi-channel receiver with flexibility in choosing center frequencies, bandwidths, and resolution is shown in Figure 3.3 [92].

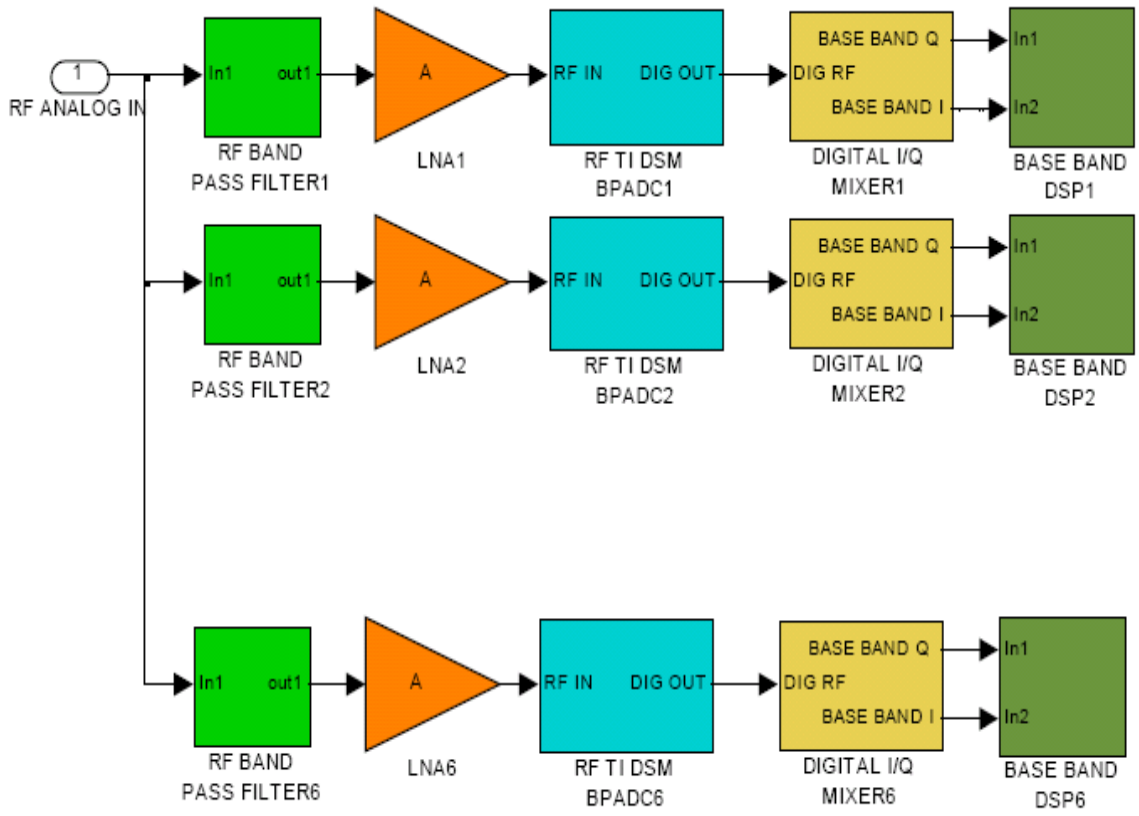

Figure 3.3 Multi-Channel Receiver with IF Band Pass ADCs

The multi-channel architecture in Figure 3.3 supports several channels with different center frequencies. For example the receiver could have six channels each with a bandwidth of 70 MHz and IF center frequencies at 1.880 GHz, 2.080 GHz, 2.280 GHz,

2.480 GHz, 2.680 GHz, 2.880 GHz. It will be shown below that a single IF Band Pass ADC design can be used for all six channels by varying the clock frequency to each of the ADCs.

3.1.3 Subsampling process

The subsampling process also called undersampling process or direct IF to digital conversion, is the process of sampling a signal outside of the first Nyquist Zone (NZ) [93]. The images will fall into the first NZ and others. The first NZ image has all the information of the signal, which can be used to restore the signal after some processing. To preserve all the signal information, the sample frequency must be greater than twice of the signal bandwidth (fb), that is fs>2fb.

Assume the signal carrier frequency is fc. To make sure fc is located at the center of a Nyquist zone, the sample frequency fs has to meet the following equation [93]:

$$fs = \frac{4fc}{2 * NZ - 1} \quad \textbf{(3.1)}$$

Where NZ=1,2,3, … and NZ corresponds to the Nyquist zone in which the carrier and its signal falls. Because the signal bandwidth fb<fs/2, any signal with frequency f would be located at frequency range of fc-fs/2 to fc+fs/2.

As seen in Equation (3.1), if NZ=1 (first Nyquist zone), then fs=4fc which meet the Nyquist criteria; if one pick NZ equals 2 (second Nyquist zone), then fs=4fc/3.

3.2 Develop Flexible BPADC Architectures to Meet Requirements of Receiver Architectures

3.2.1 Time Interleaved Delta Sigma Modulator (TIDSM) Band Pass (BP) ADC

An ADC architecture that supports IF Analog to Digital Conversion is a parallel Time Interleaved (TI) Delta Sigma Band Pass ADC [**Error! Bookmark not defined.**]. Time interleaving of ADCs is not new [94], but realizing a band pass ADC by time interleaving low pass delta sigma modulators is unique [48]. The architecture for this ADC is shown in Figure 3.4 which includes M track/hold circuits and M $\Delta\sum$ modulators in parallel, and an M+1 input multiplexer. Each $\Delta\sum$ modulator is configured to produce an N bit digital output where N is the number of quantization bits of the modulator. The multiplexer input "SELECT" control is used to select between the various N bit modulator outputs such that at any time, N bit digital outputs of one of the M modulators will flow out through the multiplexer. The switching frequency of the multiplexer is M*fs. Each track/hold circuit and its following $\Delta\sum$ modulator sample at a predetermined sample frequency fs which is a clock input signal. However each clock signal applied to its associated $\Delta\sum$ modulator is time phase shifted such that each track/hold circuit and its $\Delta\sum$ modulator samples the RF/IF analog signal at a different time, or in a time interleaved fashion, that each $\Delta\sum$ modulator output is updated in time-phased manner that corresponds to the sampling of the input signal.

Assume M channels of $\Delta\sum$ modulators are used with M clock input signals and the rising edge of the first clock signal CLK1 occurs at time t=0, each clock signal has a period of

$T = \frac{1}{fs}$. Each successive clock signal CLK2, --- CLKM is time phase shifted by $\Delta t = \frac{1}{Mfs}$. Accordingly, the mth track/hold and $\Delta\sum$ modulator receives one of the clock signals that operates at a frequency fs and time phased at $t_m = \frac{(m-1)}{Mfs}$, where m is the mth $\Delta\sum$ modulator. Each sample taken at the selected $\Delta\sum$ modulator input is $Vin(\text{mod}) = Vin(RF)\left(t + \frac{m-1}{Mfs}\right)$. The multiplexer performs an M to 1 switching of an N bit digital word. The multiplexer output is updated at a frequency of Mfs to reflect the value of the next successive $\Delta\sum$ modulator, thus the N bit multiplexer output changes at a rate of Mfs to synchronously select each time interleaved $\Delta\sum$ modulator output.

For example four parallel low pass first order delta sigma modulators operating at a sampling frequency of f_s are time interleaved, so the total effective clock frequency is 4fs. Following the previously stated criteria Equation (3.1), to make sure the carrier frequency located at the center of the Nyquist zone, $4fs = \frac{4fc}{2 * NZ - 1}$, so the center frequency fc of the band pass $\Delta\sum$ modulator is either f_s (first Nyquist zone) or $3f_s$ (second Nyquist zone) and the bandwidth is f_b. This is accomplished while preserving the increased resolution due to the over sampling and noise shaping of the low pass delta sigma modulators. Each of the four clock signals are at the same frequency fs, but the second is delayed by (1/4 Ts) relative to the first, and third is delayed by (2/4 Ts) relative to the first, and the fourth is delayed by (3/4 Ts) relative to first. The four track/hold circuits and the low pass DSMs are effectively sampling at fs. Each of the four channels incorporates a low pass DSM.

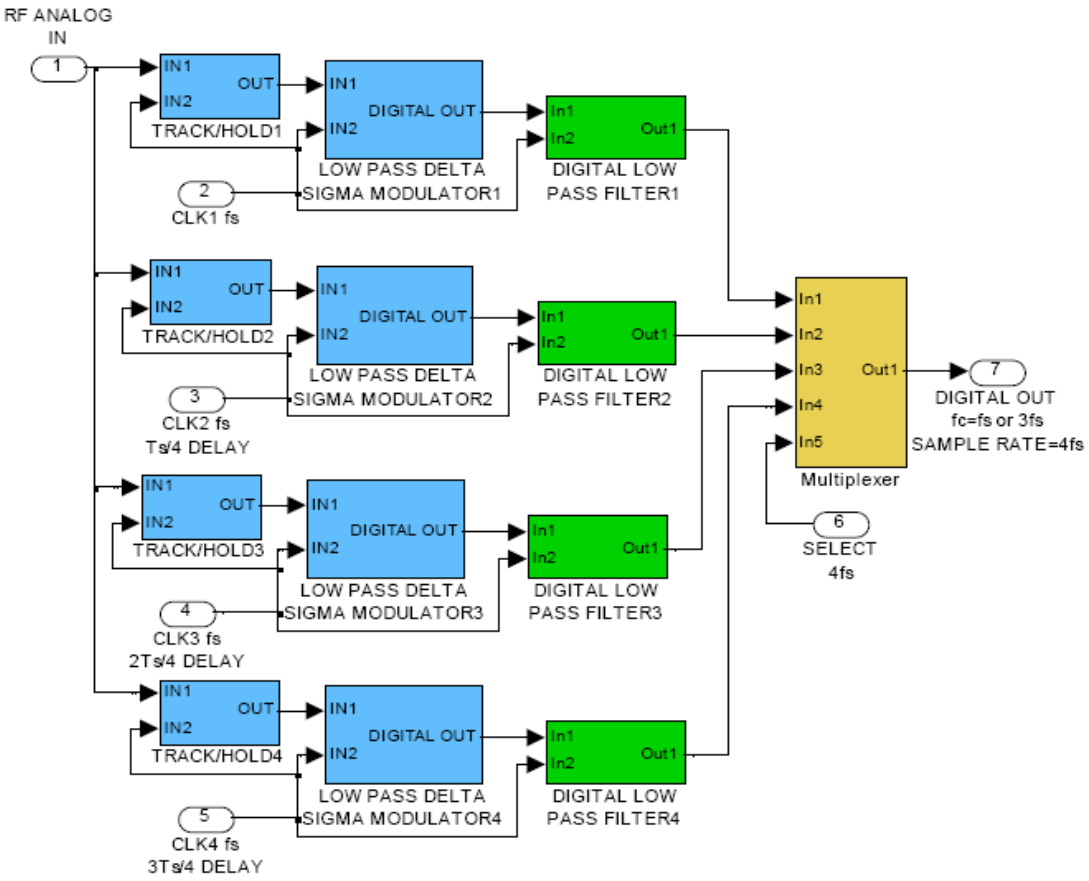

Figure 3.4 Time Interleaved Delta Sigma BPADC

As discussed in chapter 2, a low pass ADC is obtained if the N bit output of the first order modulator is passed through a digital low pass filter. The N bit output of the low pass filter has a theoretical maximum signal to noise ratio [**Error! Bookmark not defined.**]

$$\mathbf{S/N\ (db) = 6.02N-3.41+30log\ (f_s/2f_b)} \qquad \mathbf{(3.2)}$$

Where N is the number of bits produced by the quantizer and f_b is the bandwidth of the low pass filter. The effective number of bits at the output (resolution) is about equal to the signal to noise ratio divided by 6db; i.e. 6db per bit. The resolution increases by about 1.5 bits for each doubling of the over sampling ratio $f_s/2f_b$. As discussed above, the RF/IF analog input is centered at either fs (first Nyquist region) or 3fs (second Nyquist

region). Each of the modulators is sub-sampling the input since the sampling rate of fs is less than twice the input frequency. The output of each modulator is a signal at the folded frequency $|f_{in}-f_s|$ or $|f_{in}-3f_s|$. However, each of the modulator output signals in the time domain is out of phase by a time of $1/(4f_s)$. When the digital outputs of each modulator are recombined by the 4 to 1 multiplexer at the effective sampling rate of 4fs, the result is a unique digital output in the first Nyquist range (0 to 2fs) and a unique output in the second Nyquist range (2fs to 4fs). Also, the quantization noise has been shaped by the magnitude of $2\sin(\pi f/f_s)$ so that the noise is reduced to almost zero near the frequencies of fs and 3fs. The low pass filter rejects the noise outside of the bandwidth $f_b/2$, so that an increase in signal to noise ratio is obtained for a bandwidth of f_b centered at either fs or 3 fs. It can be shown that the signal to noise ratio at the output of the band pass filter is [**Error! Bookmark not defined.**]

$$\mathbf{S/N\ (db)=6.02N-6.42+30\log(f_s/\ f_b)+10\log(M)} \qquad \mathbf{(3.3)}$$

where N is the number of bits in the modulator quantizer and M is the number of modulators in parallel. For example, with N=4, fs=626.67 MHz, fb=70 MHz and M=4, the signal to noise is 58.7 db, which would result in a theoretical effective number of bits of 9.7 if the low pass filter were ideal. From the discussion above, it is seen that the Time Interleaved Delta Sigma BPADC facilitates flexibility in choosing IF center frequencies. The band pass can be centered at either fs or 3fs and can be changed over a reasonably wide range by changing fs (the sampling frequencies of the individual modulators). The resolution and bandwidth is a function of the bandwidth of the digital low pass filter as discussed above.

The digital low pass filters have a bandwidth that is one half the bandwidth of the band pass ADC. For example, if the band pass ADC is to have a bandwidth of 80 MHz, then the low pass filter should have a bandwidth of 40 MHz. The digital low pass filter can be implemented as a cascade of SINC FIR averaging filters [95] as discussed in chapter 2. A single averaging filter has the transfer function of

$$\mathbf{Tave(z)=(1/M)(1-Z^{-M})/(1-Z^{-1})} \qquad \mathbf{(3.4)}$$

The filter is implemented with M=8 and four filters are cascaded to obtain the desired attenuation in the stop band. The effective pass band for the filter is approximately fs/16. The filter is easy to implement since it requires only adders, registers and shifters as discussed in chapter 2. A compensation filter is needed at the output of the multiplexer to account for the droop due to the $Sinc^4$ filter function.

Note also that the effective sampling frequency is 4*fs, so the IF center frequency is either 4*fs/4=fs or 3(4*fs)/4=3fs. This satisfies the special case for implementing the digital I/Q without the need for multipliers as discussed previously.

3.2.2 Alternative Configuration for TI Delta Sigma BPADC

An alternative configuration for the TI Delta Sigma Band Pass ADC would have a single band pass filter after the multiplexer. This architecture is shown in Figure 3.5. For this configuration, the SINC low pass filter associated with each modulator is eliminated. A digital FIR band pass filter is used to filter the outputs of all the low pass modulators after recombining their outputs using the digital multiplexer. Comparing to the previous architecture, this TI delta sigma BPADC saves M SINC low pass filter, but the end digital band pass filter has to operate at frequency 4fs instead of fs for the M low pass

filter. 4fs would be in the range of several GHz, so implementing this filter is more of a challenge.

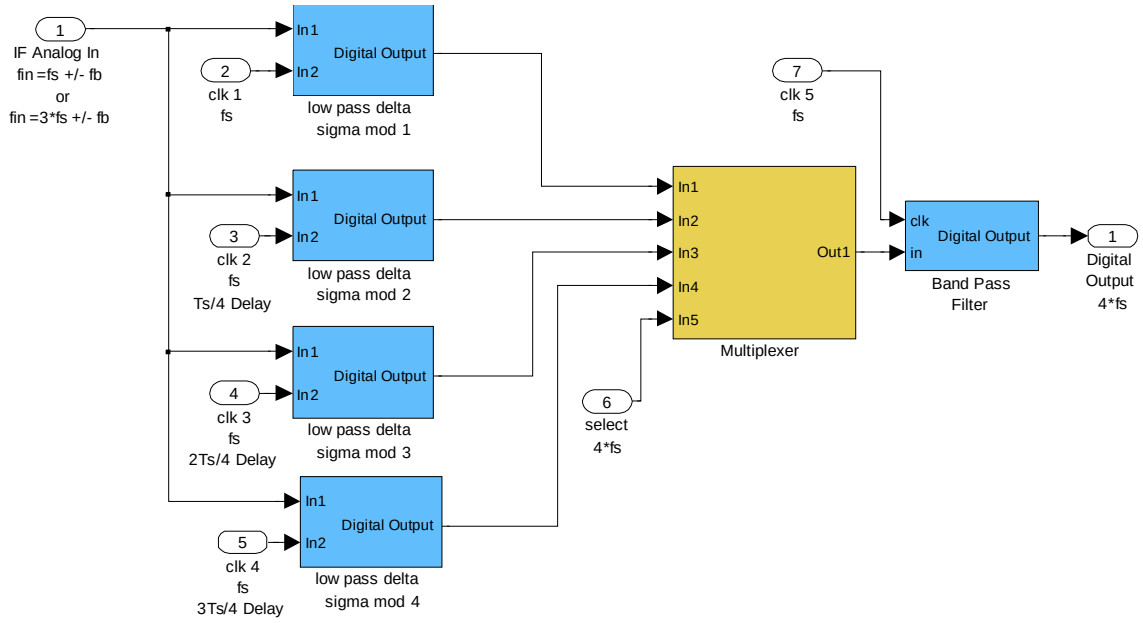

Figure 3.5 Time Interleaved Delta Sigma BPADC with Single Band Pass Filter

An FIR band pass filter was designed using the Parks-McClellen design procedure with Matlab. Since the effective sampling is 4*fs, the IF center frequency is either 4*fs/4=fs or 3(4*fs)/4=3fs. For the Parks-McClellen design algorithm the normalized frequency is the sampling frequency divided by two (Nyquist freqeucny). Thus we want the band pass to be centered at the normalized frequency of 0.5 with an effective sampling frequency of 4*fs. The frequency response for a band pass filter is shown in Figure 3.6 for an FIR filter with 200 taps and a pass band that is 0.05*2*fs. For example if fs=760 MHz, then the band width is 76 MHz.

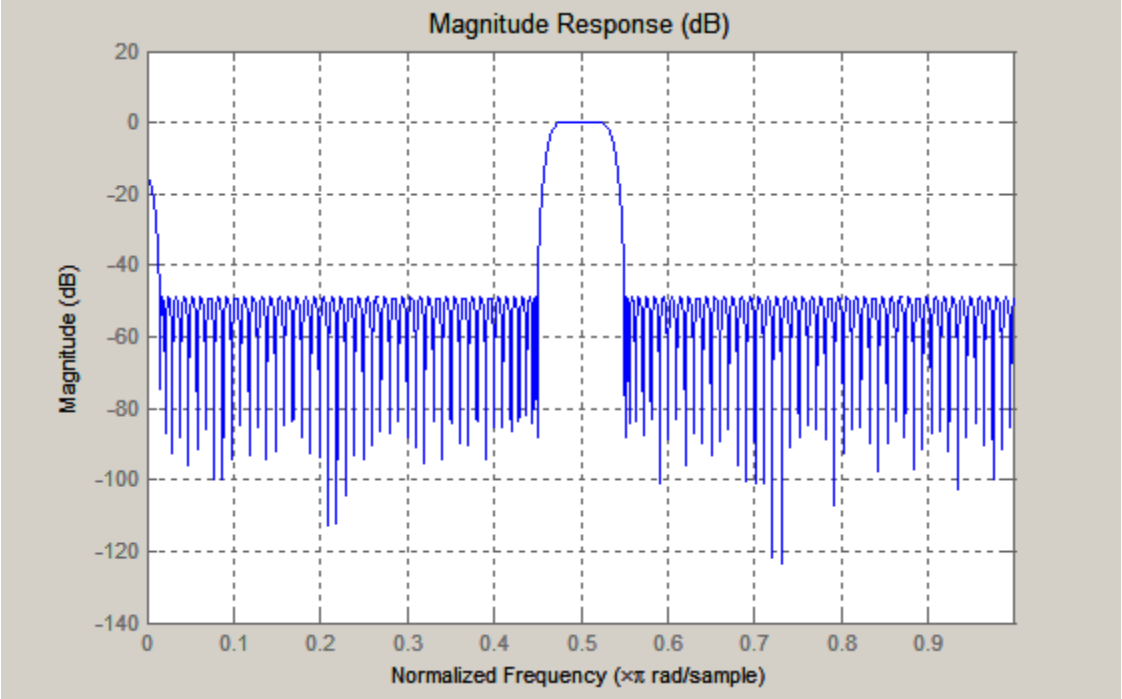

Figure 3.6 Frequency Response of FIR Band Pass Filter

For the filter response shown in Figure 3.6, the transition region between pass band and stop band has been made relatively small to help filter out the quantization noise outside the desired band. The filter response shown in Figure 3.6 is consistent with an ADC resolution of 8 bits, which will be demonstrated in a later section.

Again it is noted that the effective sampling frequency is 4*fs, so the IF center frequency is either 4*fs/4=fs or 3(4*fs)/4=3fs. This satisfies the special case for implementing the digital I/Q without the need for multipliers as discussed previously.

3.2.3 TI Delta Sigma BPADC with Pipelined Delta Sigma Modulator ADC

As discussed above, the time interleaved delta sigma band pass ADC architectures are feasible for RF/IF input signal and the resolution can be up to 8 bits with first order $\Delta\sum$ modulator 4 bit quantizer. Higher resolution can be obtained by incorporating a Pipelined

Delta Sigma Modulator (PDSM) ADC [96] as shown in Figure 3.7 below. In this figure each of the low pass delta sigma modulators and low pass filter are replaced by a PDSM ADC, which includes a low pass filter with each of the PDSM ADC channels. The PDSM ADC is given detail discussion in chapter 2.

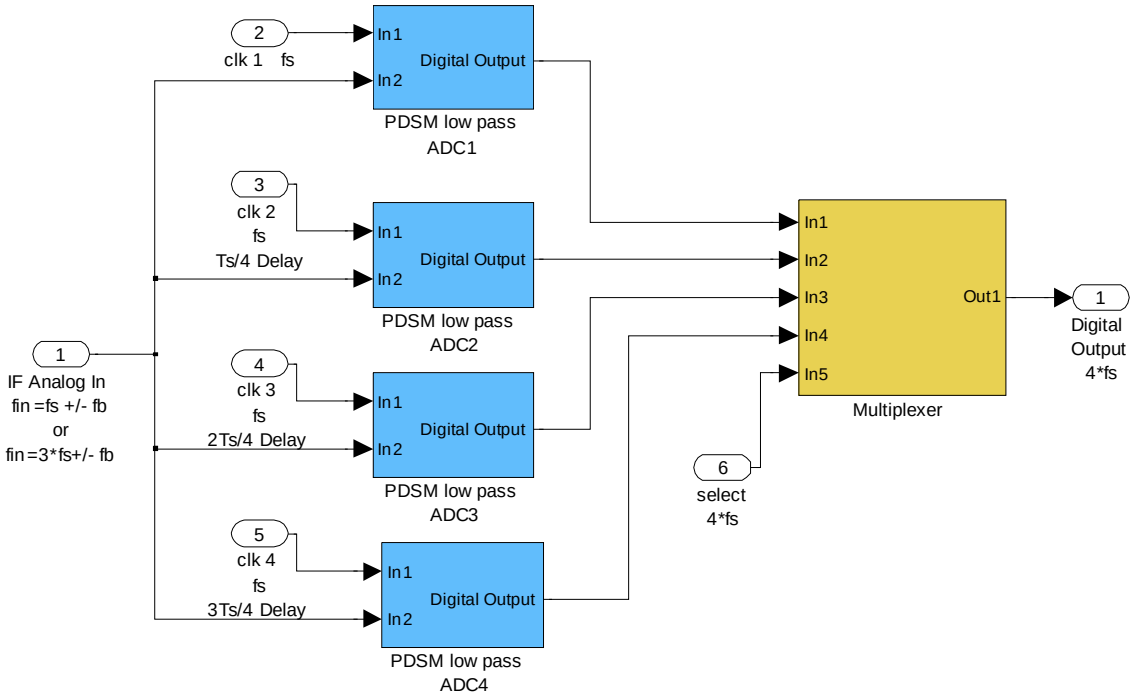

Figure 3.7 TI Delta Sigma BPADC with Pipelined Delta Sigma Modulator (PDSM) ADC

Each of the PDSM ADCs incorporates two first order low pass delta sigma modulators in a pipelined configuration as shown in Figure 3.8 below.

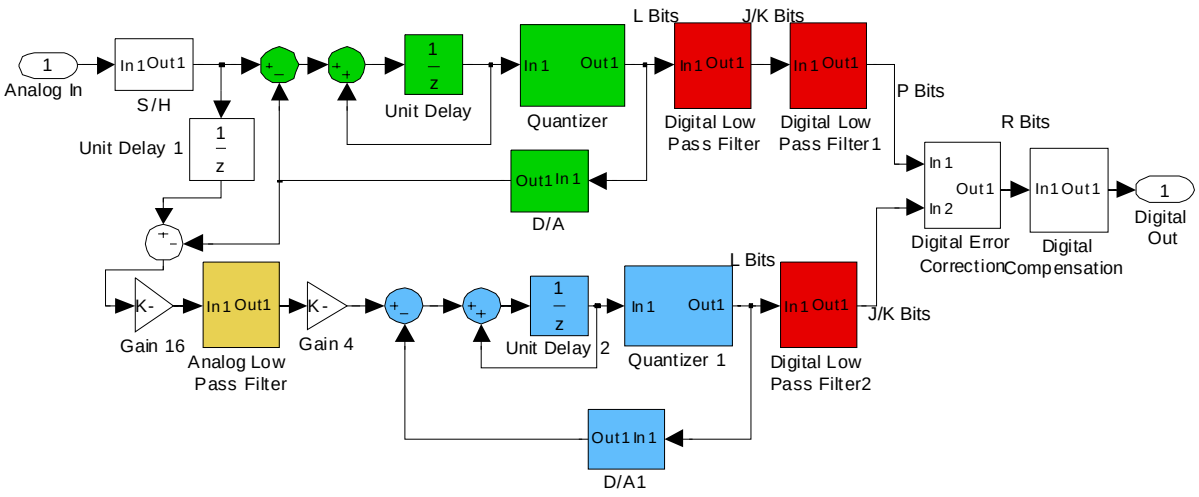

Figure 3.8 Pipelined Delta Sigma Modulator (PDSM) ADC Architecture

As seen in Figure 3.8, the first stage of the PDSM ADC is a standard first order delta sigma modulator with a discrete integrator, multi-bit quantizer, and a two stage low pass filter. A four bit quantizer is used for this implementation and the clock frequency (fs). The four bit output of the quantizer is passed through two stages of low pass filtering. The low pass filters are SINC averaging filters which implement the function $T_{ave}(z) = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i}$ as discussed in chapter 2. After filtering, the digital output of the first stage is a 13 bit word. The 13 bit digital output is only accurate to 7-8 bits with an oversampling ratio (OSR) of 8. The resolution of the first stage would increase with a higher OSR. Again referring to Figure 3.8, the input to the second stage is the difference between the analog input (after a clock delay) and the analog version of the output of the first stage quantizer. This analog error signal is then put through an analog low pass filter that has the same sampled data transfer function as the digital low pass filters for stage one. The magnitude of the in band signals are attenuated by the $(\text{Sinc})^2$ function and must be precisely offset by the compensation filter after combining the first and second

stage digital outputs. After passing though the analog low pass filter, the high frequency components of the error signal are attenuated, leaving a predominantly low frequency error signal that is amplified so that the dynamic range is the same as the analog input signal. The filtered and amplified error signal is the input to the second stage first order modulator and digital low pass filter as seen in Figure 3.8. The digital output of the second stage digital filter (which is again a cascade of two Sinc averaging filters) is the digital version of the error signal. The digital word is 10 bits wide, but only accurate to 6-7 bits. The digital outputs of the first stage and second stage are combined with the proper weighting to obtain an output that theoretically should be accurate to 14-15 bits for a two stage PDSM ADC. As mentioned above the, compensation filter must precisely offset the in band attenuation due averaging filters. Note that both the first stage output and the second stage output is subjected to the same total filter transfer function of $(Sinc)^4$.

As discussed in chapter 2, the MatLab simulation shows that two stage PDSM ADC can reach up to 13-16 bit resolution with 1GHz clock frequency and 62.5 MHz input bandwidth. Cadence simulation shows the PDSM ADC is able to get 12-13 bit resolution with the same set up as MatLab. So time interleaving four PDSM ADC as shown in Figure 3.7 will get 12-13 bits output with RF/IF input.

3.2.4 Multi-Channel Receiver with TI Delta Sigma Band Pass ADCs

The TI Delta Sigma Band Pass ADCs have the flexibility for implementing the Multi-Channel Receiver discussed above. Assume the receiver has six channels each with a bandwidth of 80 MHz and IF center frequencies at 1.880 GHz, 2.080 GHz, 2.280 GHz, 2.480 GHz, 2.680 GHz, 2.880 GHz. This can be implemented with six TI Sigma Delta

Band Pass ADCs with the low pass modulators and low pass filters sampling at f_{s1}=1.880GHz/3=626.667 MHz, f_{s2}=2.080GHz/3=693.333 MHz, f_{s3}=2.280GHz/3=760 MHz, f_{s4}=2.480GHz/3=826.667 MHz, f_{s5}=2.680GHz/3=893.333 MHz, and f_{s6}=2.880GHz/3=960 MHz. With this choice of sampling frequencies for the modulators and filters, the IF center frequencies would be at 3fs. This corresponds to the second Nyquist region of the effective sampling rate of 4fs. It can be seen that the center frequency is changeable by adjusting the clock frequency and each channel receiver can receive different carrier signal with its associated flexible clock frequency. In the next section, the performance of the TI Sigma Delta Band Pass ADCs operating at these frequencies will be assessed using Matlab/Simulink.

3.3 Assess Performance of Selected BPADC Architectures

3.3.1 Matlab Results for Multi-Channel Receiver with TI Delta Sigma Band Pass ADCs

The TI Delta Sigma Band Pass ADC design with four first order delta sigma modulator and cascaded low pass Sinc filters in parallel was captured using Simulink/Matlab as shown in Figure 3.9. The first order delta sigma modulator and four cascaded low pass Sinc filters discussed in the previous section was modeled as shown in Figure 3.10. The first order delta sigma modulator is composed of an integrator and a four bit quantizer, which is modeled by Simulink/Matlab as seen in Figure 3.11. Each of the cascaded low pass filters is implemented as Figure 3.12.

The results of simulations are presented below for Multi-Channel Receiver example. The results are given for the lowest center frequency (1880 MHz), a middle center frequency

(2280 MHz), and the highest center frequency (2880 MHz). Figure 3.9 shows the TI Delta Sigma Band Pass ADC for an IF input that is centered at 1880 MHz and a bandwidth of 70 MHz. The 70 MHz bandwidth is obtained using the four cascaded Sinc filters each of length 8 as shown in Figure 3.12. For this case, the modulators and low pass filters are sampling at frequency of 626.667 MHz (1880/3 MHz) and the clock delay between two consecutive interleaved modulators is Ts/4=0.3989 ps. The effective sampling frequency is 4*626.667=2.50667 GHz. The IF center frequency of 1880 MHz is at 3*626.667 and is in the second Nyquist region.

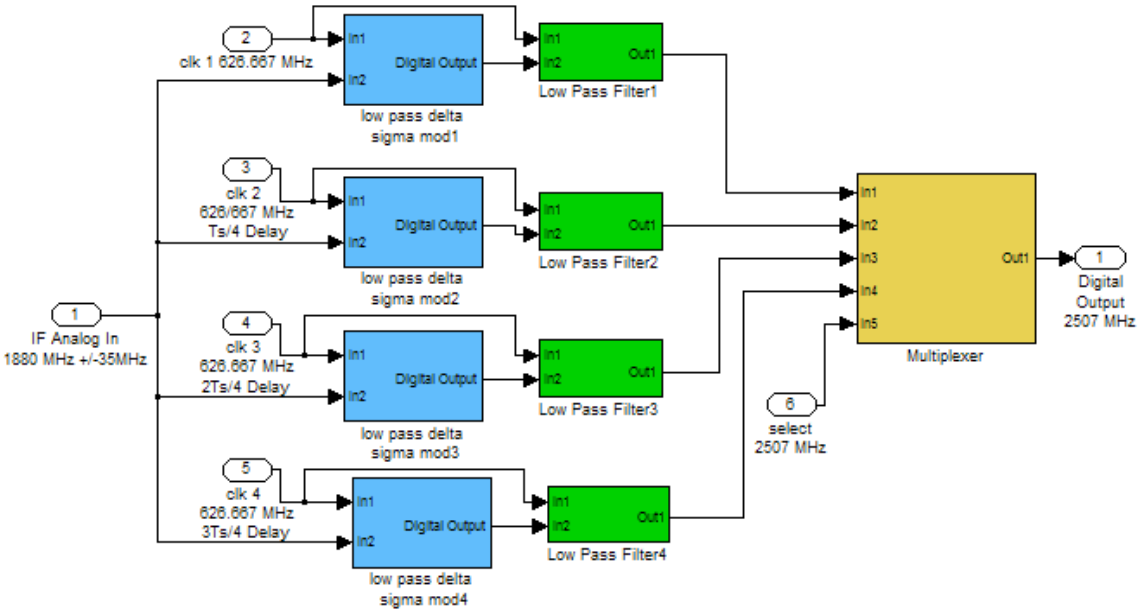

Figure 3.9 TI Delta Sigma Band Pass ADC with 1880 MHz Center Frequency

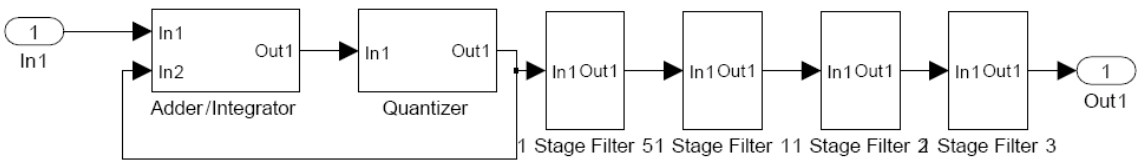

Figure 3.10 Single Low Pass Delta Sigma Modulator and Cascaded Low Pass Filter Block Diagram

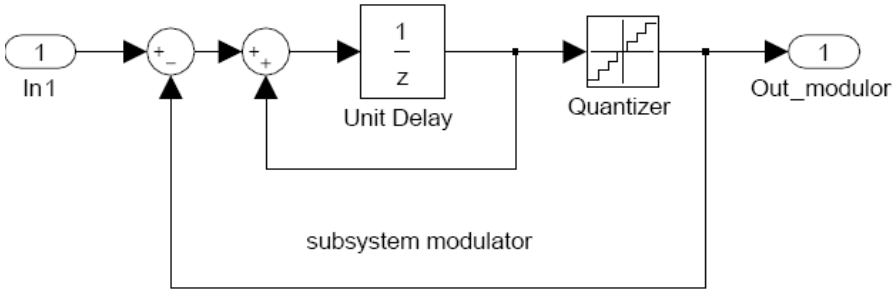

Figure 3.11 First Order Delta Sigma Modulator Simulink Model

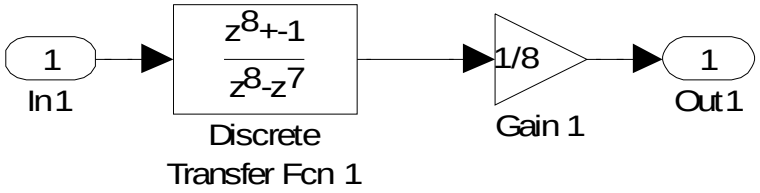

Figure 3.12 One Stage Low Pass Filter Simulink Model

The Band Pass ADC of Figure 3.9 was simulated with an input signal of 1885 MHz. The FFT of the output is shown in Figure 3.13 below.

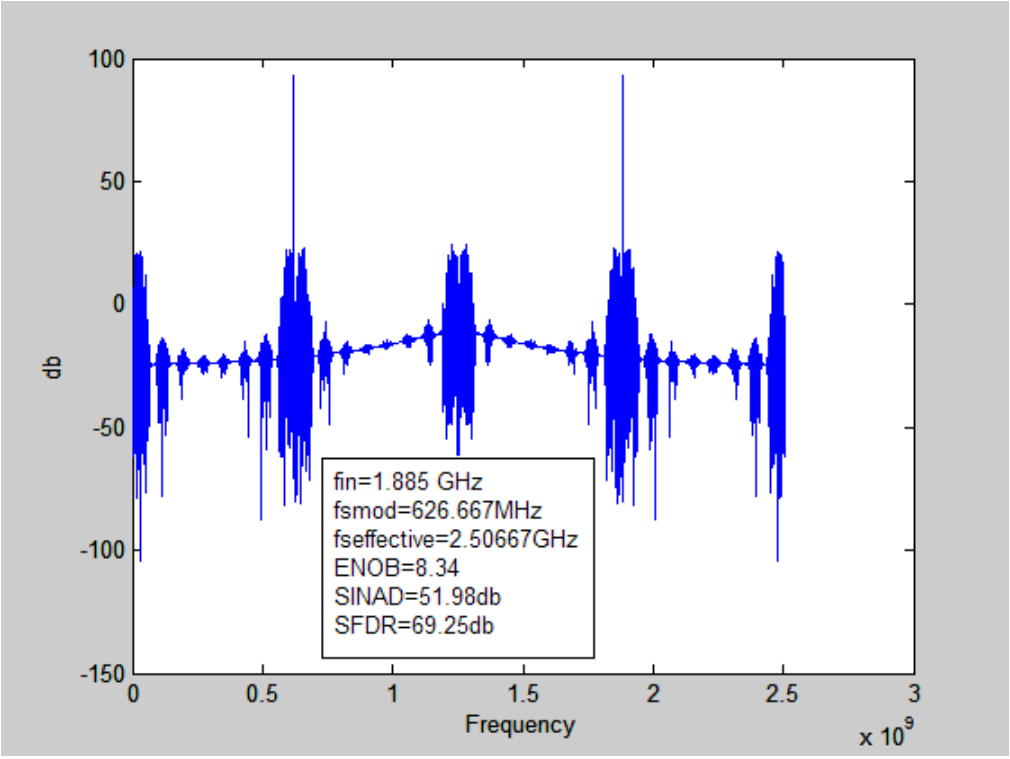

Figure 3.13 FFT Results for TI BP ADC
fcenter=1880 MHz BW=70 MHz fin=1885 MHz

The FFT results show a unique signal corresponding to the input at 1885 MHz in the second Nyquist region and a unique signal at the first Nyquist region which is |4fs-fin|=621.67 MHz. After recombining the outputs of the time interleaved modulators and filters, the low pass filters yield an effective band pass filter centered at 626.667 MHz and 3*626.667 MHz. So the signal (and noise) is passed near 626.667 MHz and 1880 MHz as is seen in Figure 3.13. The filters have an effective bandwidth of about 70 MHz and the signal to noise and distortion (SINAD) of 51.98 db indicates an Effective Number of Bits (ENOB) of 8.34.

Figure 3.14 shows the TI Delta Sigma Band Pass ADC configured for an IF analog input centered at 2280 MHz, which corresponds to the middle channels of the multi-channel receiver. In this case the modulators and digital low pass filters are clocked at 760 MHz ($fs=f_{center}/3$), and the effective sampling frequency at the output of the multiplexer is 3.04 GHz (4fs). Figure 3.15 shows the FFT results for an input of 2285 MHz. The FFT results indicate that the signal and noise are passed for frequencies of 2280+/-35 MHz. The delta sigma modulators reduce the quantization noise in near 2280 MHz, so the signal to noise and distortion ratio (SINAD) for this case is 52.56 db. This corresponds to an effective number of bits (ENOB) of 8.44.

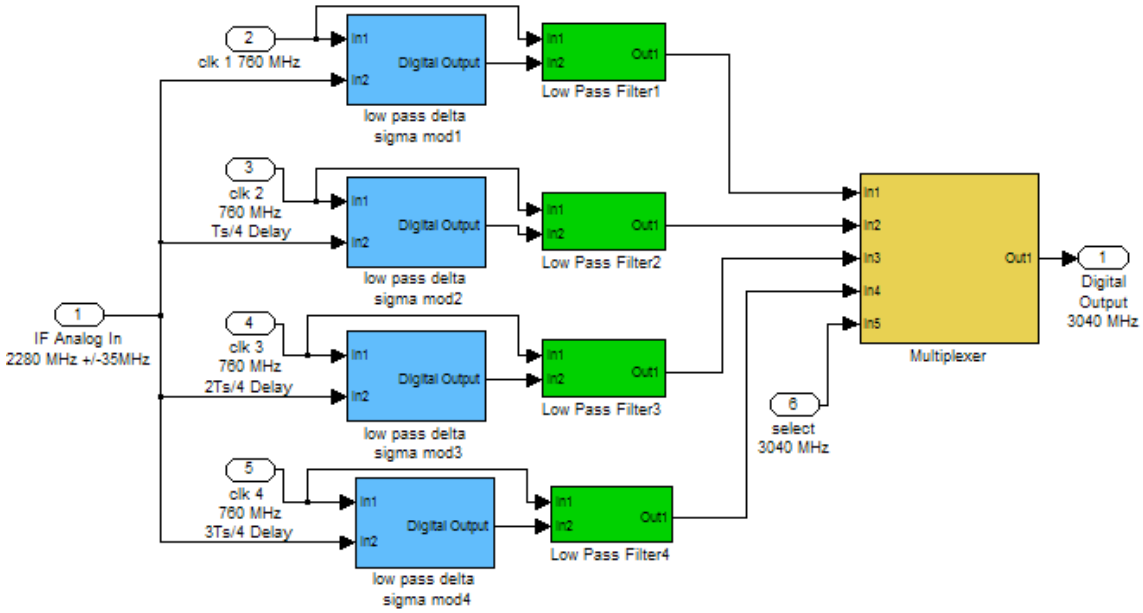

Figure 3.14 TI Delta Sigma Band Pass ADC with 2280 MHz Center Frequency

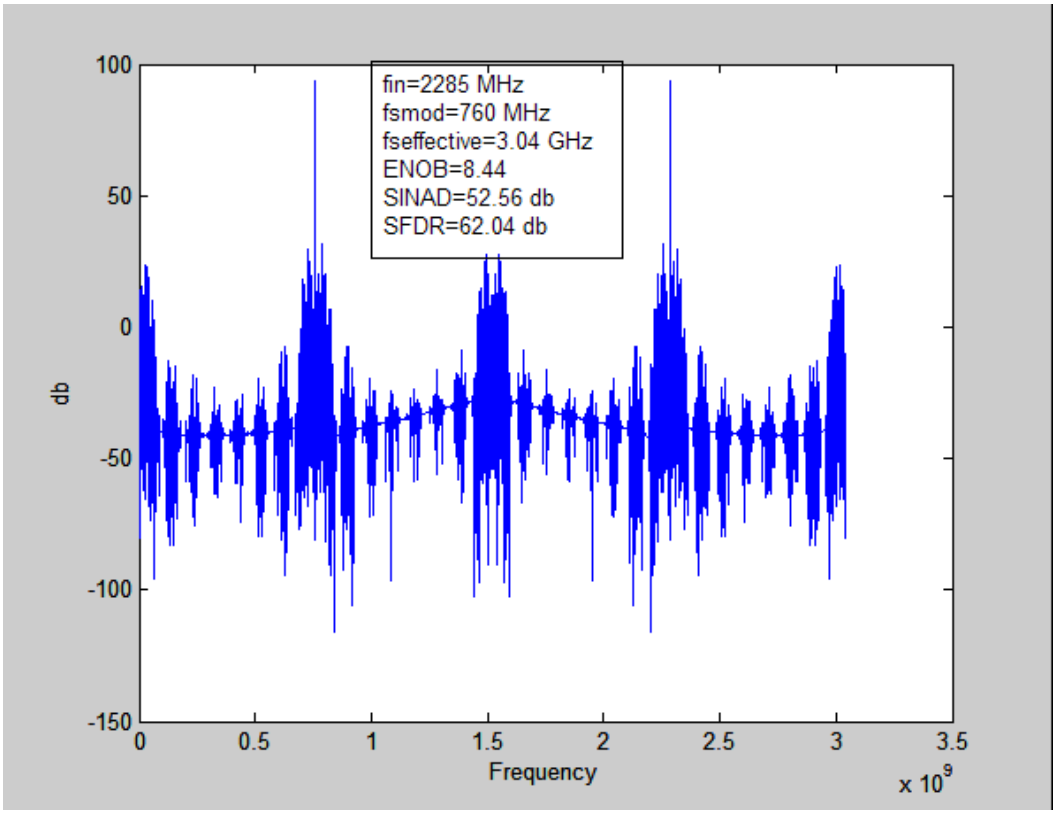

Figure 3.15 FFT Results for TI BP ADC

fcenter=2280 MHz BW=70 MHz fin=2285 MHz

Figure 3.16 shows the TI Delta Sigma Band Pass ADC configured for a center frequency of 2880 MHz, which is the highest center frequency for the multi-band receiver example. In this case the modulators and low pass filters are clocked at 960 MHz ($fs=f_{center}/3$), which gives an effective sampling frequency of 3.84 GHz (4*fs). The FFT results for an input of 2885 MHz is shown in Figure 3.17. The SINAD and ENOB for this case are 53.99 db and 8.68 respectively.

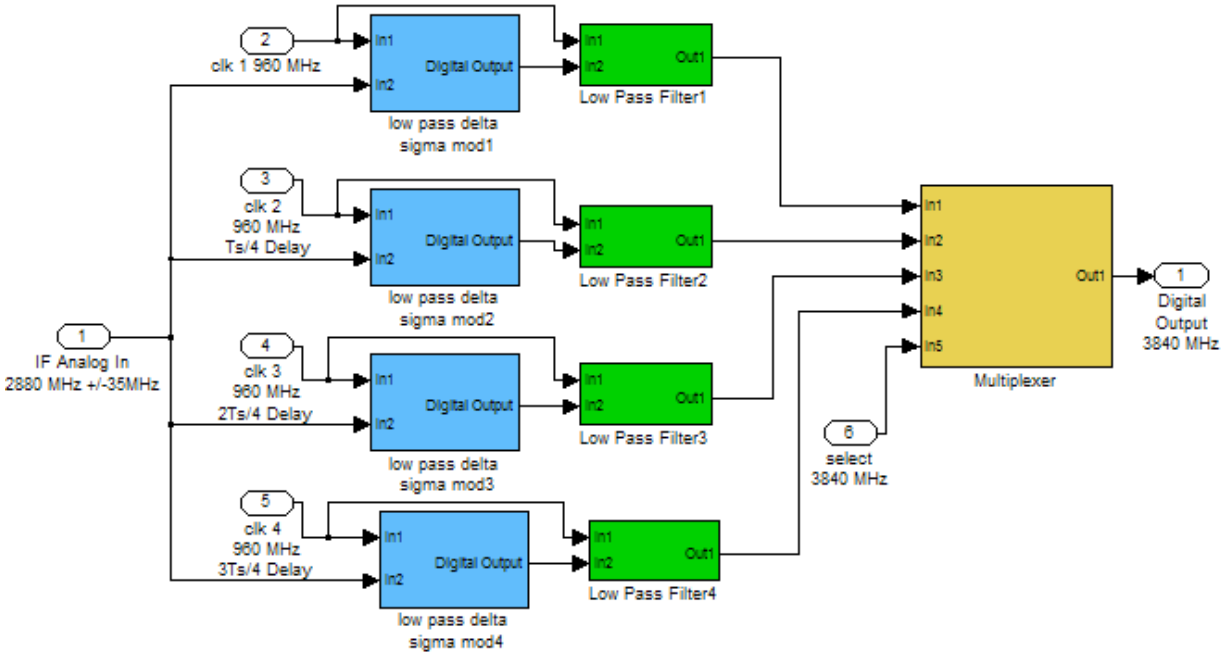

Figure 3.16 TI Delta Sigma Band Pass ADC with 2880 MHz Center Frequency

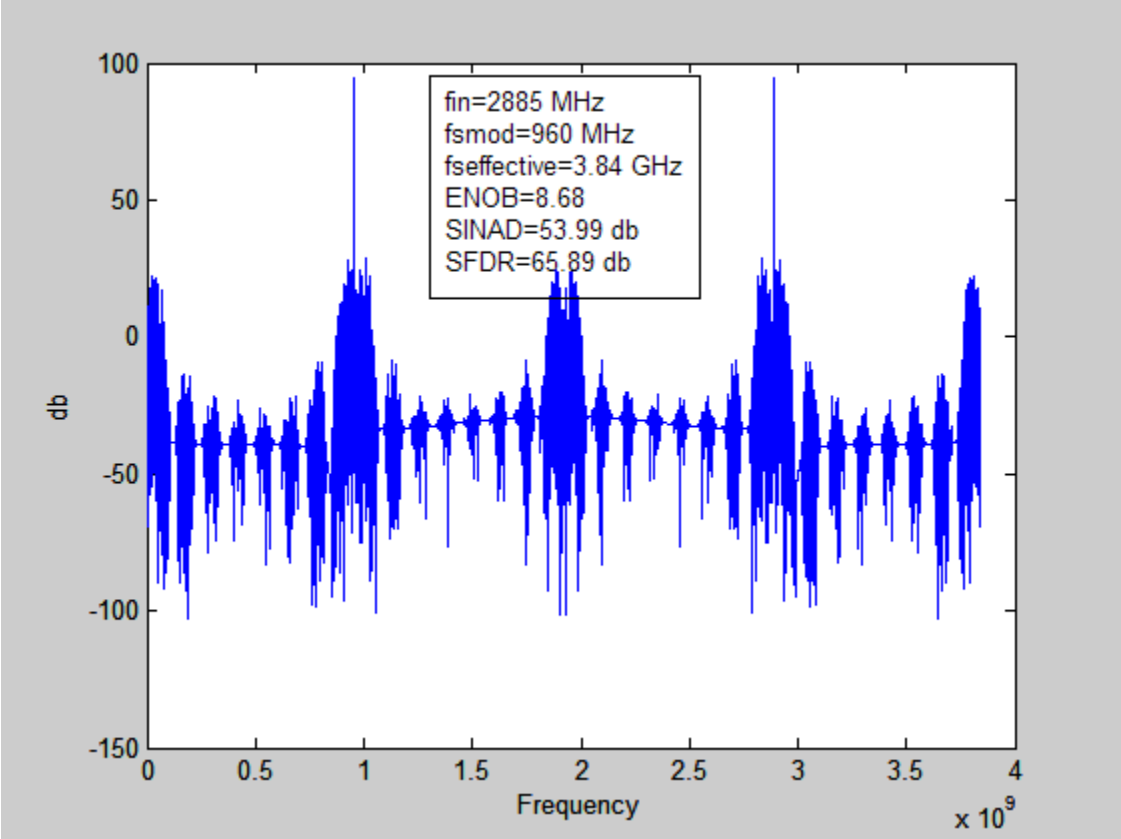

Figure 3.17 FFT Results for TI BP ADC

fcenter=2880 MHz BW=70 MHz fin=2885 MHz

3.3.2 Matlab Results for Multi-Channel Receiver with TI Delta Sigma Band Pass ADCs Using Band Pass Filters

As discussed above, the TI Delta Sigma Modulator Band Pass ADC can be configured with one band pass filter, rather than having a low pass filter in each of the four channels. Figure 3.18 shows the TI Delta Sigma Band Pass ADC for an IF input that is centered at 1880 MHz and a bandwidth of 70 MHz. The 70 MHz bandwidth is obtained using the single band pass FIR filter which is implemented by using Parks-McClellan optimal FIR filter design "firpm" function. For this case, the modulators are sampling at frequency of 626.667 MHz and the clock delay between interleaved modulators is Ts/4=0.3989 ps.

The band pass filter is sampling at the effective sampling frequency which is 4*626.667=2.50667 GHz. The IF center frequency of 1880 MHz is at 3*626.667 and is in the second Nyquist region. The band pass FIR filter has 200 symmetrical coefficients as shown in Table 3.1

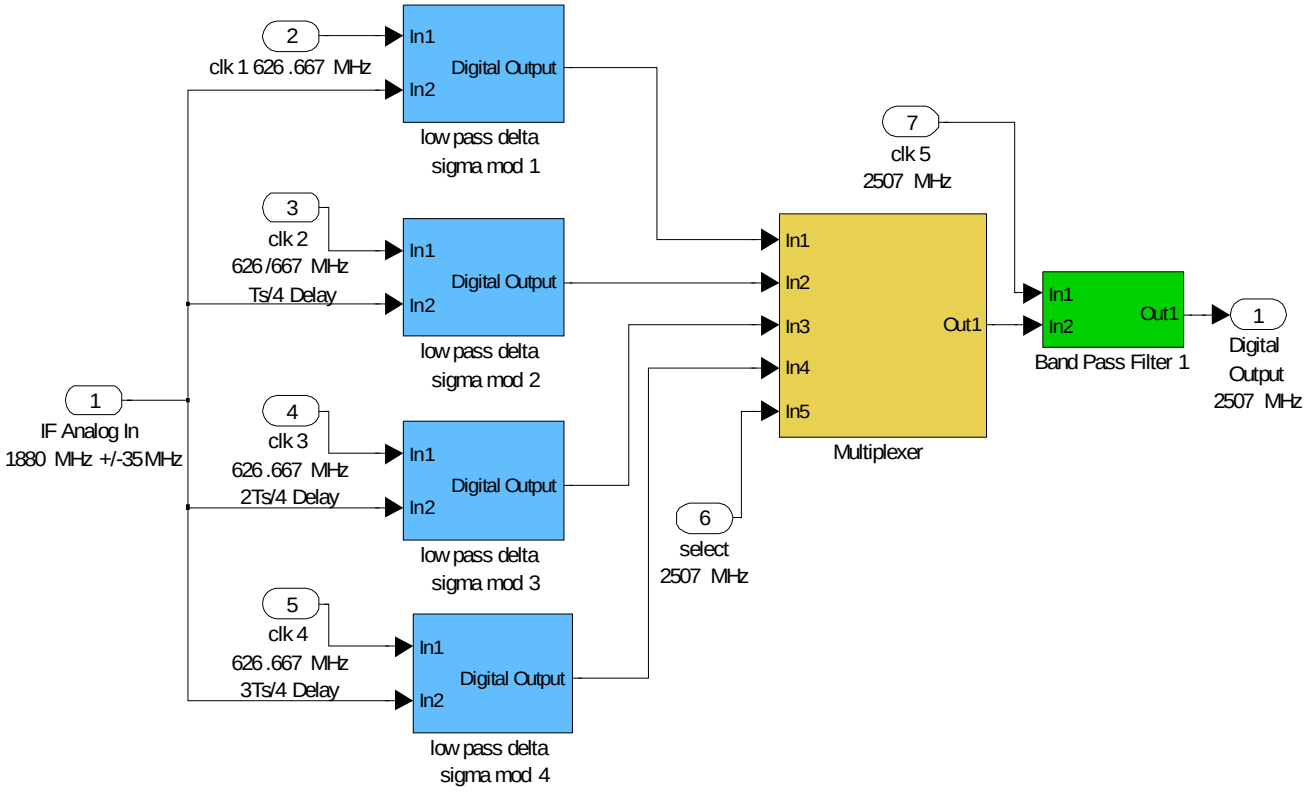

Figure 3.18 TI Delta Sigma Band Pass ADC with Single Band Pass Filter with 1880MHz Center Frequency

Table 3.1 Band Pass Filter Coefficients

[0.0001 0.0001 0.0024 0.0002 -0.0010 0.0002 0.0016 0.0002 -0.0012 0.0003 0.0018 0.0003 -0.0011 0.0003 0.0016 0.0003 -0.0006 0.0004 0.0009 0.0004 0.0004 0.0004 -0.0003 0.0004 0.0019 0.0005 -0.0018 0.0005 0.0035 0.0005 -0.0032 0.0006 0.0049 0.0006 -0.0041 0.0006 0.0055 0.0007 -0.0040 0.0007 0.0048 0.0007 -0.0026 0.0007 0.0028 0.0008 0.0003 0.0008 -0.0005 0.0008 0.0042 0.0009 -0.0046 0.0009 0.0085 0.0009 -0.0086 0.0010 0.0122 0.0010 -0.0114 0.0010 0.0140 0.0010 -0.0118 0.0011 0.0129 0.0011 -0.0088 0.0011 0.0081 0.0011 -0.0019 0.0012 -0.0006 0.0012 0.0088 0.0012 -0.0129 0.0012 0.0224 0.0012 -0.0275 0.0012 0.0377 0.0013 -0.0427 0.0013 0.0525 0.0013 -0.0566 0.0013 0.0650 0.0013 -0.0672 0.0013 0.0733 0.0013 -0.0729 0.0013 0.0762 0.0013 -0.0729 0.0013 0.0733 0.0013 -0.0672 0.0013 0.0650 0.0013 -0.0566 0.0013 0.0525 0.0013 -0.0427 0.0013 0.0377 0.0012 -0.0275 0.0012 0.0224 0.0012 -0.0129 0.0012 0.0088 0.0012 -0.0006 0.0012 -0.0019 0.0011 0.0081 0.0011 -0.0088 0.0011 0.0129 0.0011 -0.0118 0.0010 0.0140 0.0010 -0.0114 0.0010 0.0122 0.0010 -0.0086 0.0009 0.0085 0.0009 -0.0046 0.0009 0.0042 0.0008 -0.0005 0.0008 0.0003 0.0008 0.0028 0.0007 -0.0026 0.0007 0.0048 0.0007 -0.0040 0.0007 0.0055 0.0006 -0.0041 0.0006 0.0049 0.0006 -0.0032 0.0005 0.0035 0.0005 -0.0018 0.0005 0.0019 0.0004 -0.0003 0.0004 0.0004 0.0004 0.0009 0.0004 -0.0006 0.0003 0.0016 0.0003 -0.0011 0.0003 0.0018 0.0003 -0.0012 0.0002 0.0016 0.0002 -0.0010 0.0002 0.0024 0.0001]

Figure 3.19 shows the FFT results for an input of 1890 MHz. The FFT results indicate that the signal and noise are passed for frequencies of 1880+/-35 MHz. The delta sigma modulators reduce the quantization noise in near 1880 MHz, so the signal to noise and

distortion ratio (SINAD) for this case is 50.55 db. This corresponds to an effective number of bits (ENOB) of 8.11.

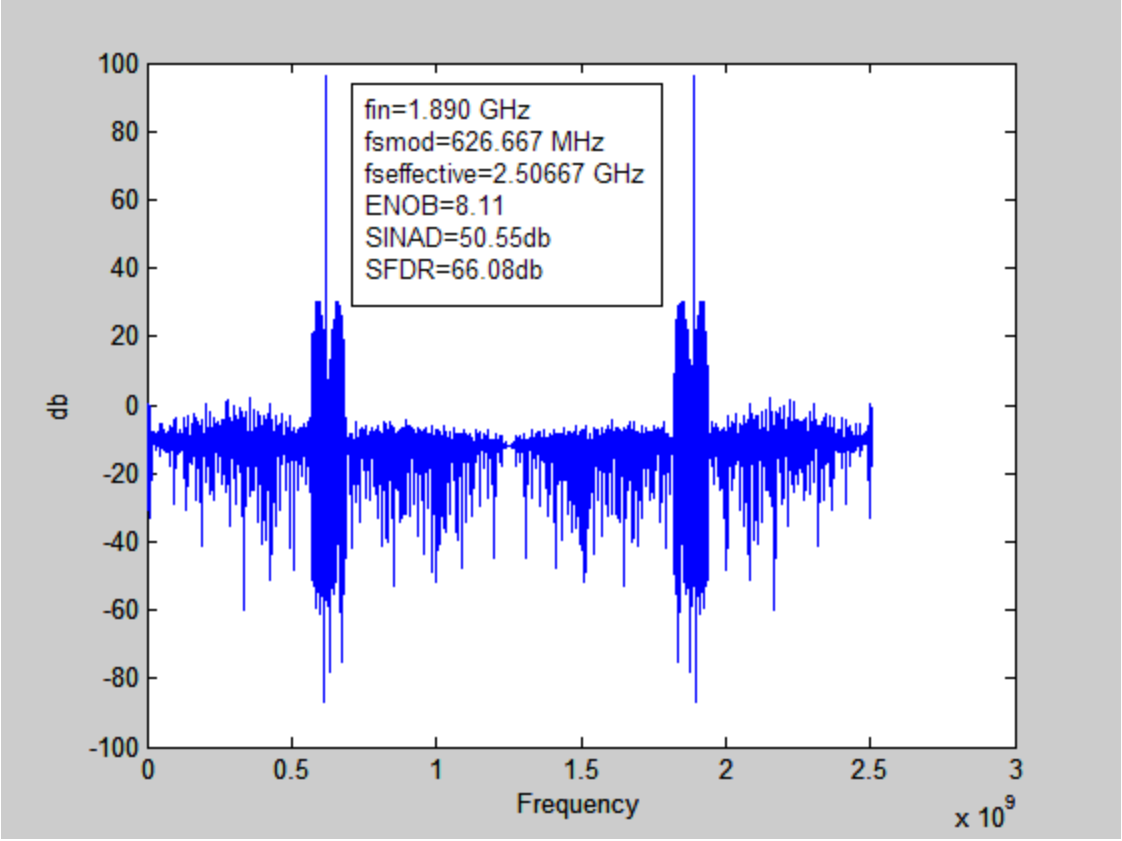

Figure 3.19 FFT Results for TI BP ADC Single Band Pass Filter fcenter=1880 MHz BW=70 MHz fin=1890 MHz

FFT results are shown in Figure 3.20 and Figure 3.21 for the TI BPADC using a single band pass filter for center frequencies of 2280 MHz and 2880 MHz respectively.

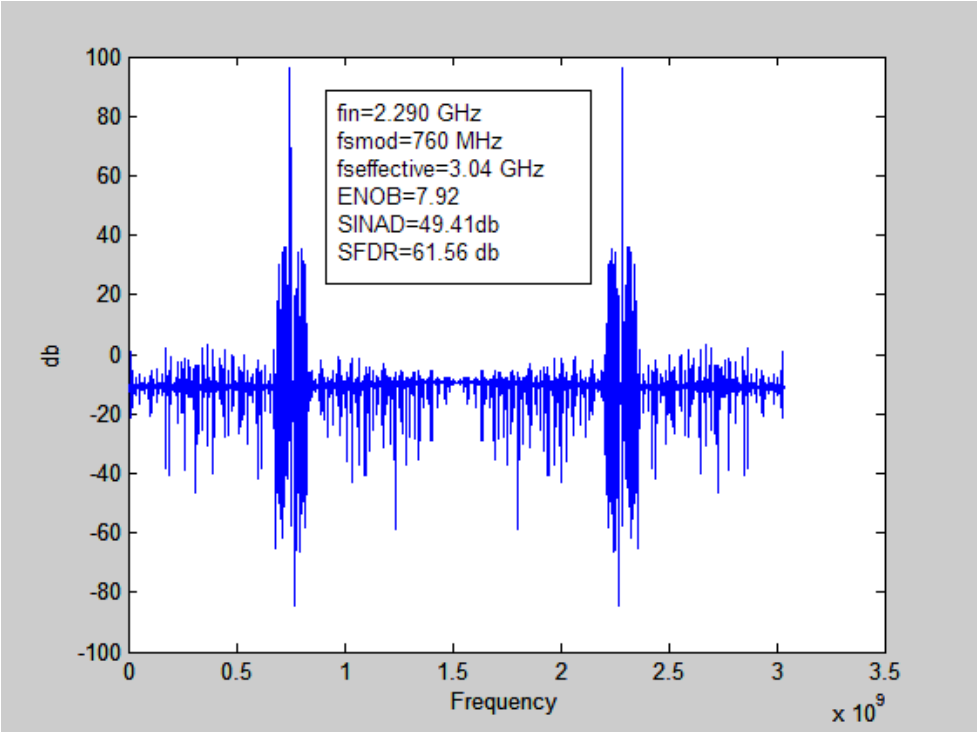

Figure 3.20 FFT Results for TI BP ADC Single Band Pass Filter fcenter=2280 MHz BW=70 MHz fin=2290 MHz

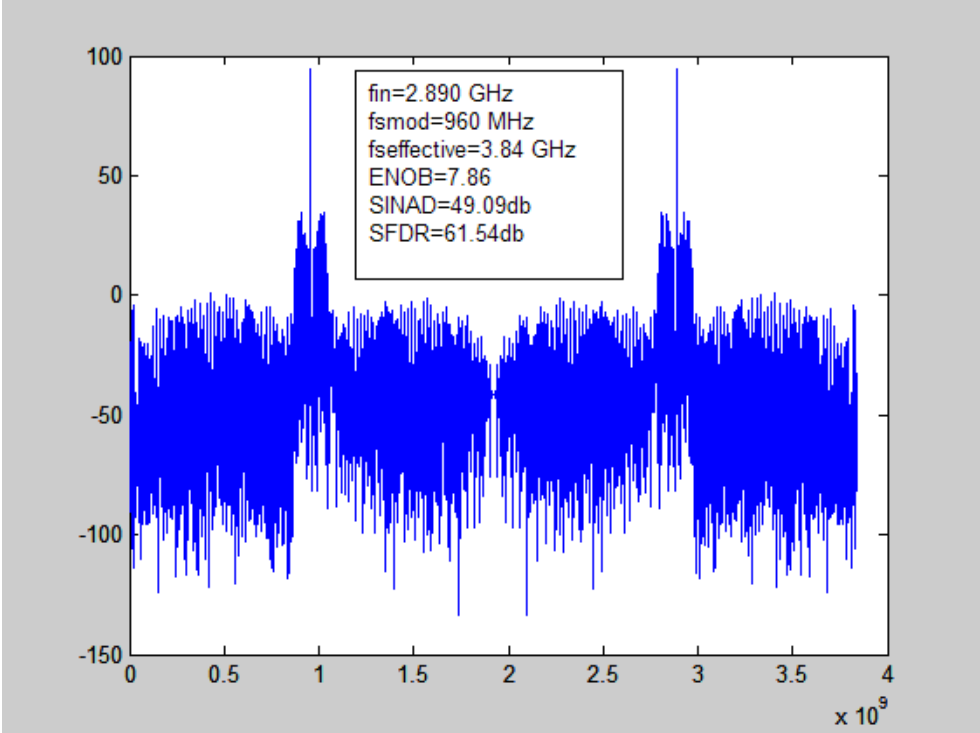

Figure 3.21 FFT Results for TI BP ADC Single Band Pass Filter fcenter=2880 MHz BW=70 MHz fin=2890 MHz

3.3.3 Matlab Results for Multi-Channel Receiver with TI Delta Sigma BPADC with Pipelined Delta Sigma Modulator ADC

Resolution can be significantly increased for the same bandwidth by using a Pipelined Delta Sigma Modulator (PDSM) ADC as described in the previous section. Figure 3.22 shows a TI Delta Sigma BPADC using a PDSM ADC in each channel. Each Channel single two stage PDSM ADC is captured by Simuilnk/Matlab as shown in Figure 3.23 which includes two stage first order delta sigma modulator and four cascaded low pass Sinc filters as discussed in previous sections.

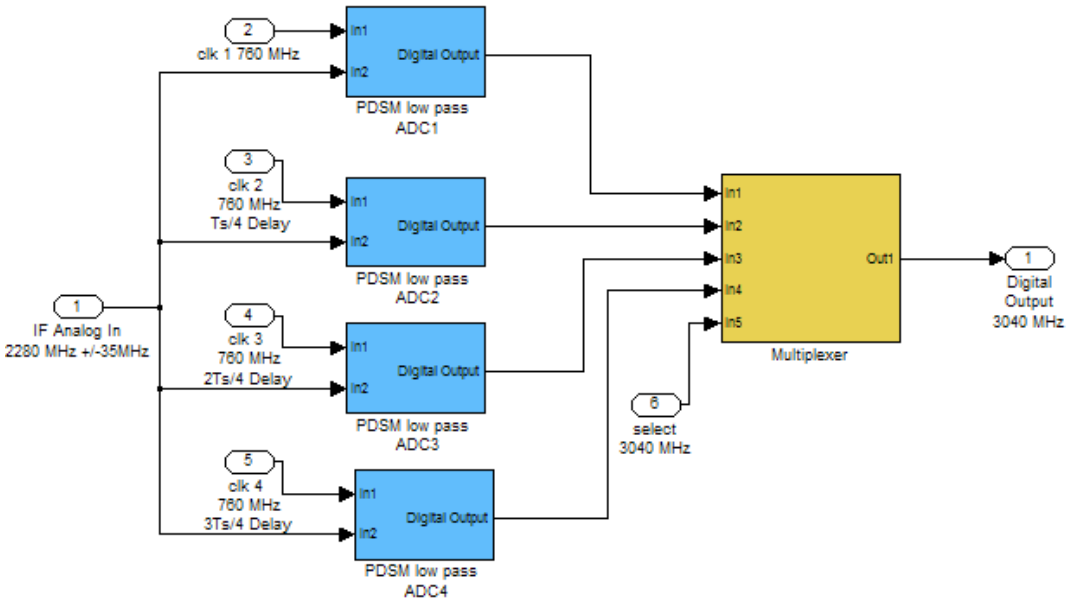

Figure 3.22 TI Delta Sigma Band Pass ADC with PDSM Low Pass ADC with 2280MHz Center Frequency

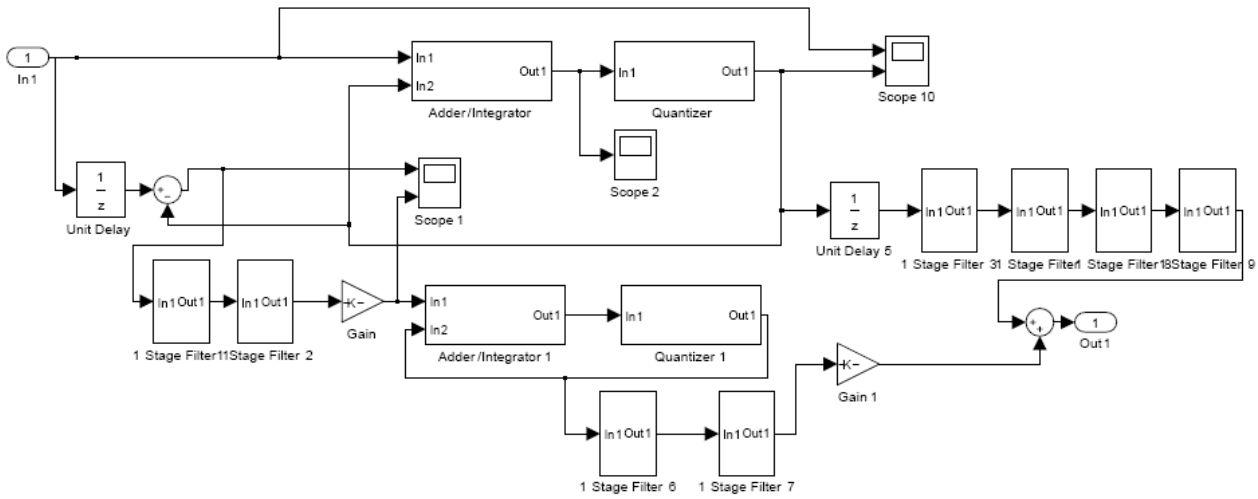

Figure 3.23 Two Stage PDSM ADC Simulink Model

Figure 3.24 shows the FFT results for the TI BPADC using the PDSM Low Pass ADCs with a center frequency of 2280 MHz. The signal to noise ratio is significantly increased to 95.28 db and the effective number of bits is 15.09.

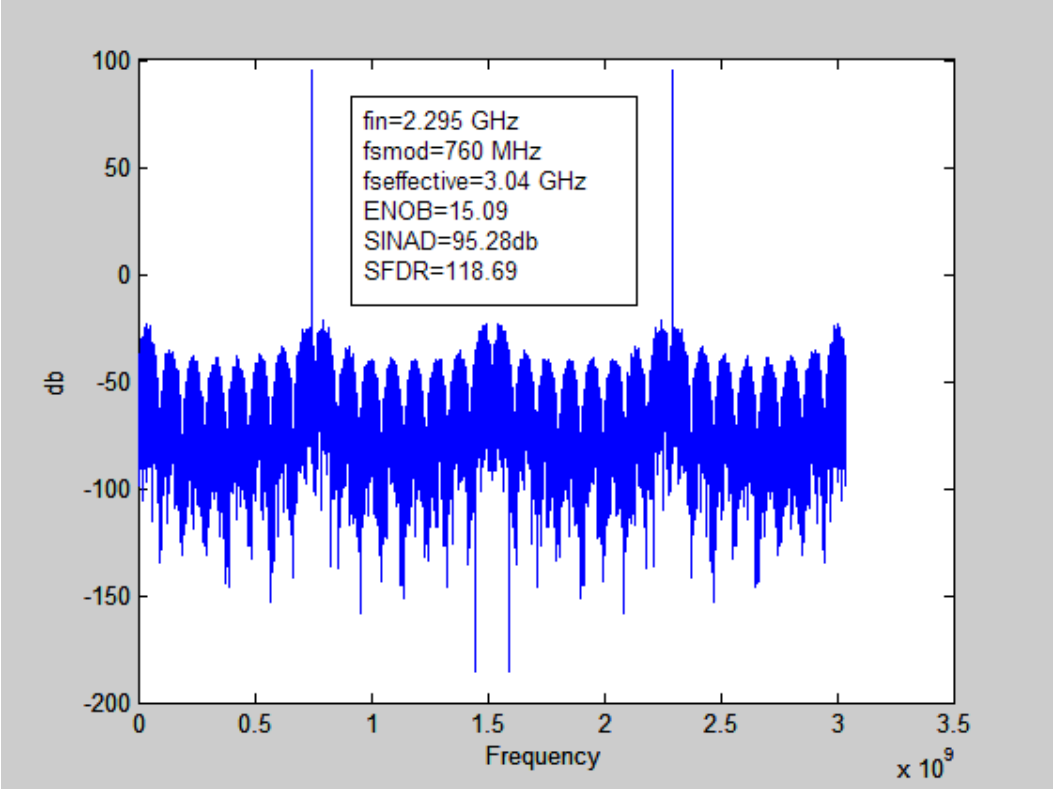

Figure 3.24 FFT Results for TI BP ADC PDSM ADC in each Channel fcenter=2280 MHz BW=70 MHz fin=2295 MHz

Table 3.2 gives the summary of the TI DSM BP ADCs performances.

Table 3.2 Summary of TI DSM BP ADCs Performances

Architecture	fin (GHz)	fin (GHz)	fb (MHz)	fs (MHz)	f_{eff} (GHz)	SINAD (db)	SFDR (db)	ENOB
TI BPADC/LP Filters	1.88	1.885	70	626.667	2.50667	51.98	69.26	8.34
TI BPADC/BP Filter	~	1.89	~	~	~	50.55	66.08	8.11
TI BPADC/LP Filters	2.28	2.285	70	760	3.04	52.56	62.04	8.44
TI BPADC/BP Filter	~	2.29	~	~	~	49.41	61.56	7.92
TI BPADC/PDSM	~	2.295	~	~	~	95.28	118.69	15.09
TI BPADC/LP Filters	2.88	2.885	70	960	3.84	53.99	65.89	8.68
TI BPADC/BP Filter	~	2.89	~	~	~	49.09	61.54	7.86

Note: fin is the input frequency; fs is the sample frequency of each modulator; f_{eff} is the effective sample frequency of the ADC; the delta-sigma modulator quantizer resolution is 4 bit.

3.4 Conclusions

This chapter presents a unique TI DSM BPADC which integrated with an RF receiver front end to achieve RF/IF A/D data conversion and I/Q down conversion with a simplified digital mixer. The Simulink/Matlab simulation results show the following features of this TI DSM BPADC.

- The results presented for the TI Delta Sigma Band Pass ADC show that the architecture supports flexible IF center frequencies without changes in hardware.
- Center frequencies are modified by changing the clock frequency of the modulator, low pass filter and multiplexer.

- The resolution is determined by the modulator clock frequency and the bandwidth of the low pass (band pass) filters. The resulting bandwidth (fb) of the band pass ADC is twice that of the low pass filter centered at either fs (first Nyquist region) or 3fs (second Nyquist region).
- More resolution is obtained if the ratio of fs/fb is increased.
- The multi-channel receiver architecture was used as an example and demonstrated the flexibility of the TI Delta Sigma Band Pass ADC.
- The TI Delta Sigma Band Pass ADC allows a tradeoff between bandwidth and resolution. For resolutions of above 8 bits application, the ration of 4fs/fb must be larger than 10.
- An alternative configuration for the TI Delta Sigma BPADC was defined that used only a single band pass filter, rather than a low pass filter in each channel. The performance for the two configurations was about the same. The single band pass filter may save some hardware, but it must be clocked at 4*fs rather than fs.
- A Pipelined Delta Sigma Modulator (PDSM) ADC can be used in place of the Low Pass Delta Sigma Modulator to increase resolution for a given over sampling ratio. The resolution is increased with the cost of additional hardware and complexity.

In summary, the combination of time interleaving with delta sigma modulation results in relatively high RF/IF center frequencies and good resolution with relatively low component clock frequencies. Sampling frequencies for the track/hold, modulators and low pass filters of less than 1 GHz support RF center frequencies up to 3 GHz. The relatively low sample rates facilitate an ASIC implementation in CMOS technology.

4 On Chip Clock Design

Any ADC system would require sample hold circuit(s) and register latch(s), which will be controlled by the clocks. As the required ADCs bandwidth and resolution increase, the clock accuracy becomes very critical to the system. Clean and low jitter clock sources must be employed on chip. This chapter is going to present some alternative implementations of on chip clock generators that include the CMOS VCO, CMOS Phase Locked Loops and CMOS Delayed Locked Loops.

4.1 Introduction

Three alternative implementations of an on chip clock source are the inverter ring oscillator, Voltage Controlled Oscillator (VCO) and Phase Lock Loop (PLL) synthesizer.

4.1.1 Inverter Ring Oscillator

The typical and easiest clock generator is the inverter ring oscillator which has an odd number of inverter gain stages in a ring. For an n stage inverter ring oscillator, the period of the oscillator is $T=2N*\tau_D$ and frequency is $f = \frac{1}{T} = \frac{1}{2N * \tau_D}$, where N has to be greater than one odd integer, τ_D is an inverter gate delay. Figure 4.1 [97] shows a three stage inverter ring oscillator and its associated time delay and each stage output signal sequence. The oscillator frequency will totally depend on the inverter gate delays which will vary with different loading and fabrication technologies, so it is hard to predict a

precise frequency of operation after fabrication. Another disadvantage of the inverter ring oscillator is its poor phase noise performance.

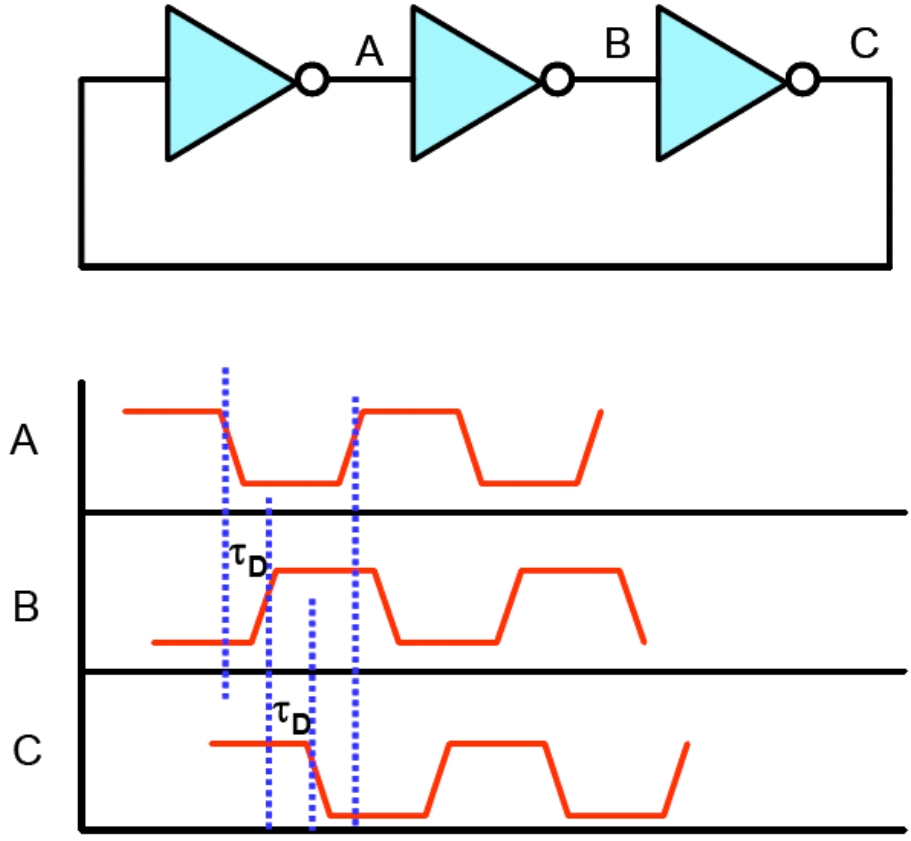

Figure 4.1 Three Stage Inverter Ring Oscillator Block Diagram and Time Sequence

4.1.2 Voltage Control Inverter Ring Oscillator

The voltage control inverter ring oscillator also called current-starved VCO [98] is similar to the inverter ring oscillator, which include an odd number of inverters. Unlike the inverter ring oscillator, the voltage control oscillator has a DC voltage input to control the current of the inverters, so to control the charging and discharging capacitor speed, and thus to control the oscillating frequency. The oscillating frequency of this VCO is [98]

$$f_{osc} = \frac{1}{N.C_{tot}.Vdd} \tag{4.1}$$

Where N is the number of stages, usually is bigger than 5; Ctot is the total capacitance of each stage inverter which includes both input and output capacitance of the inverter. Vdd is the power supply. This architecture is power hungry, so it is usually suited for low oscillating frequency to keep low power dissipation.

4.1.3 Voltage Control Wide Range Oscillator

Another VCO is a transconductor based VCO with wide range and high stability which was first published in 1952 [99,100]. The fundamental concept is that the oscillator frequency would be able to be tuned in a wide range instead of single frequency and also increases the stability. The voltage control wide range oscillator can be used for both high and low frequency application.

4.1.4 Phase Lock Loop (PLL)

PLLs are the most popular types of clock generators which can lock the clock phase based on the precise low frequency crystal reference clock. For some of the high resolution ADC applications, it requires a very stable clock supply, so the Phase Lock Loop (PLL) will be the most popular clock source. The time interleaved ADC as discussed in chapter3 requires the stable phase shifted clock to each of the four channels, so a four phase shifted clocks (In phase and Quadrature clocks) will be investigated in the following sections.

The following efforts associated with CMOS on chip clock implementations are presented in this chapter:

- Investigate a voltage control wide range oscillator centered at 1 GHz frequency, including schematic, layout design and fabrication with the ADC.
- Investigate Phase Lock Loop synthesizer architectures which will be able to generate In phase and Quadrature four phase clock. Two architectures are studied: one is Time Interleaved Delay-Locked Loop Clock Generator; another is PLL with Dual Delay Voltage Control Oscillator (VCO).

4.2 A Voltage Control Wide Range Oscillator Design

A 12 bit 1GHz/s with 62.5MHz bandwidth ADC is discussed in chapter 2. A very critical component is the on chip clock generator. The desired operating frequency is 1.0 GHz, but an on chip clock with a wide range of operating frequencies is desirable for testing at low frequencies. Several wide range VCO on chip clock sources were designed with frequency range of 4 MHz to 1.1 GHZ, 360 MHz to 1.36 GHz, 400 MHz to 2.63 GHz and 879 MHz to 4.1 GHz. These designs and performances are presented below.

4.2.1 Basic VCO with wide operating range architecture

The basic VCO with wide range operating architecture is shown in Figure 4.2 [101], where the magnitudes of the current sources are controlled by an external voltage (vcontrol), and are proportional to (VDD-vcontrol) based on the P-channel current source. The positive feedback around the loop is used to ensure that only one of M0 and

M1 are on at one time. The switching points of the inverters combined with the current source determine the oscillating frequency [102].

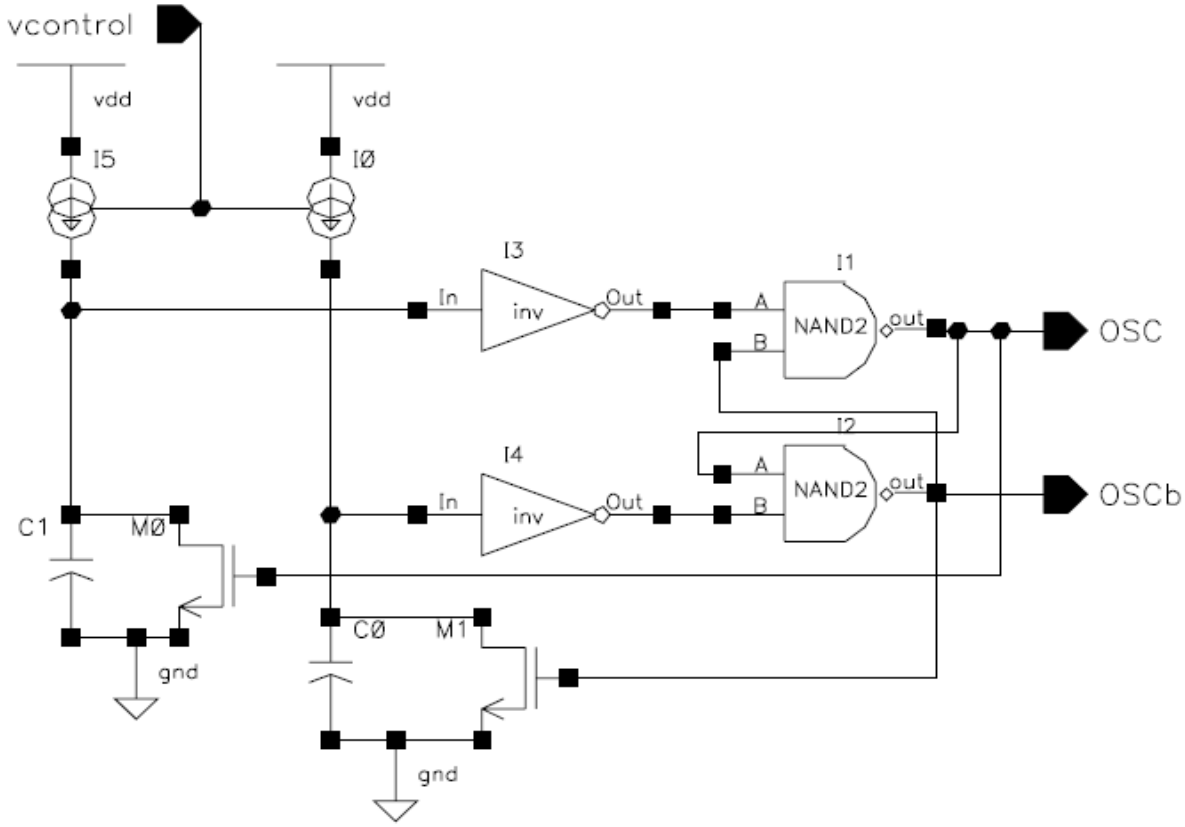

Figure 4.2 Wide Range VCO Block Diagram

The voltage waveform is shown in Figure 4.3. As seen in Figure 4.3, when output signal "OSC" is low and "OSCb" is high, M1 will be on and M0 will be off, so the drain voltage of M0 (Vds0) is going to be charged toward to VDD through a equivalent capacitor which is composed of capacitor C1, transistor M0 drain to bulk capacitance Cdb0 and the gate capacitance Cgs of inverter I3, so the Ctotal=C1+Cdb0+Cgs3, where both Cdb0 and Cgs3 are proportional to the related transistor sizes. The time for charging Ctotal to Vsp is given by

$$t1' = Ctotal\frac{Vsp}{I5} \quad \textbf{(4.2)}$$

where Vsp is called switching point voltage. The switching point voltage is the point where the input voltage equals the output voltage. The drain to source voltage of transistor M1, Vds1 is discharged to ground since M1 is on. As Vds0 approaches Vsp, the output of the inverter I3 is falling toward Vsp and will reach ground after a gate delay (t_{delay1}). As long as the output of the I3 is less than Vsp, the output (OSC) of the NAND gate (I1) is reset back to high after a NAND gate delay (t_{delay2}). The total time for OSC remaining low will be

$$\Delta t = t1 - t0 = t' + t_{delay1} + t_{delay2} = Ctotal\frac{Vsp}{I5} + t_{delay1} + t_{delay2} \quad \textbf{(4.3)}$$

The same analysis applies to M1. So the VCO oscillating frequency is $f_{osc} = \frac{1}{2.\Delta t}$ which is widely dependant on the current source I5 if the sizes of the transistors and the number of gates are fixed. The current source is controlled by the DC control input. To get a higher oscillating frequency, it requires larger source current and also smaller capacitance and less gate delays. As mentioned above, the current source is implemented by the P-channel transistors whose gate is connected to the DC voltage control input. As the control voltage increases, the source to gate voltage (Vsg=VDD-vcontrol) is reduced. The lower current source results in the oscillating frequency getting smaller. If all the hardwares are kept unchanged, reducing the vcontrol voltage will result in increasing the oscillating frequency.

This basic wide range VCO architecture is used to implement a 150 MHz to 1.1 GHz on chip clock source. The details are discussed in the following sections.

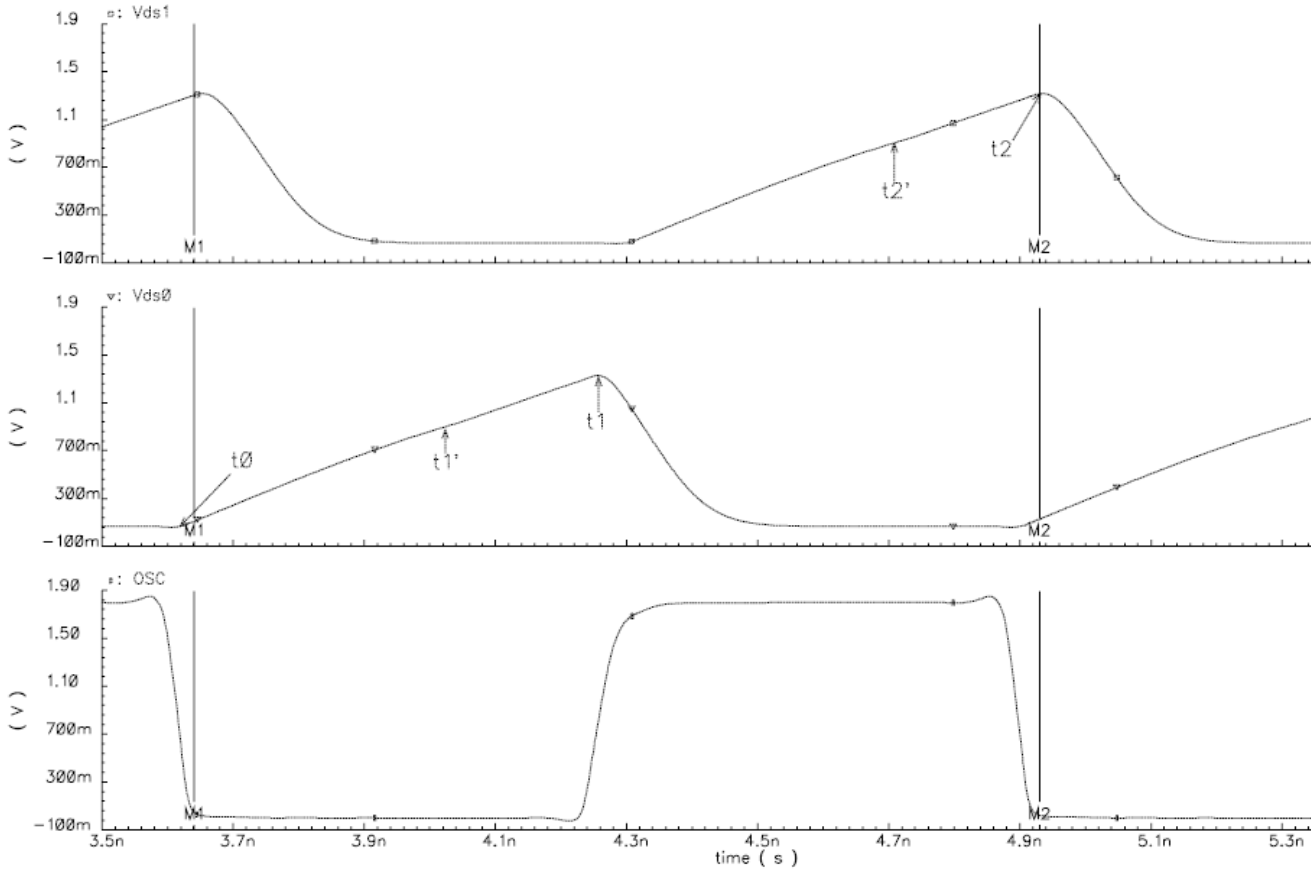

Figure 4.3 Voltage Waveform of Figure 4.2 for Wide Range VCO

Top Figure: Drain to Source Voltage verses Time of Transistor M1 on Figure 4.2

Middle Figure: Drain to Source Voltage verses Time of Transistor M0 on Figure 4.2

Bottom Figure: Wide Range VCO Oscillating Output

4.2.2 Wide Range VCO designs using TSMC 0.18um CMOS process

The VCO with wide range operating is designed using TSMC 0.18 um CMOS process, the top level schematic circuit is shown in Figure 4.4. As discussed above, to get the specified frequency f_{osc}, it requires $2\Delta t$ to be $1/ f_{osc}$ within the resolution error. As seen from equation (4.2), the frequency will not only rely on the current source and the capacitance, but also depends on the gate delays, so some combinations of the three

factors are needed to meet the requirement. The following sections will give some detailed discussions and design examples.

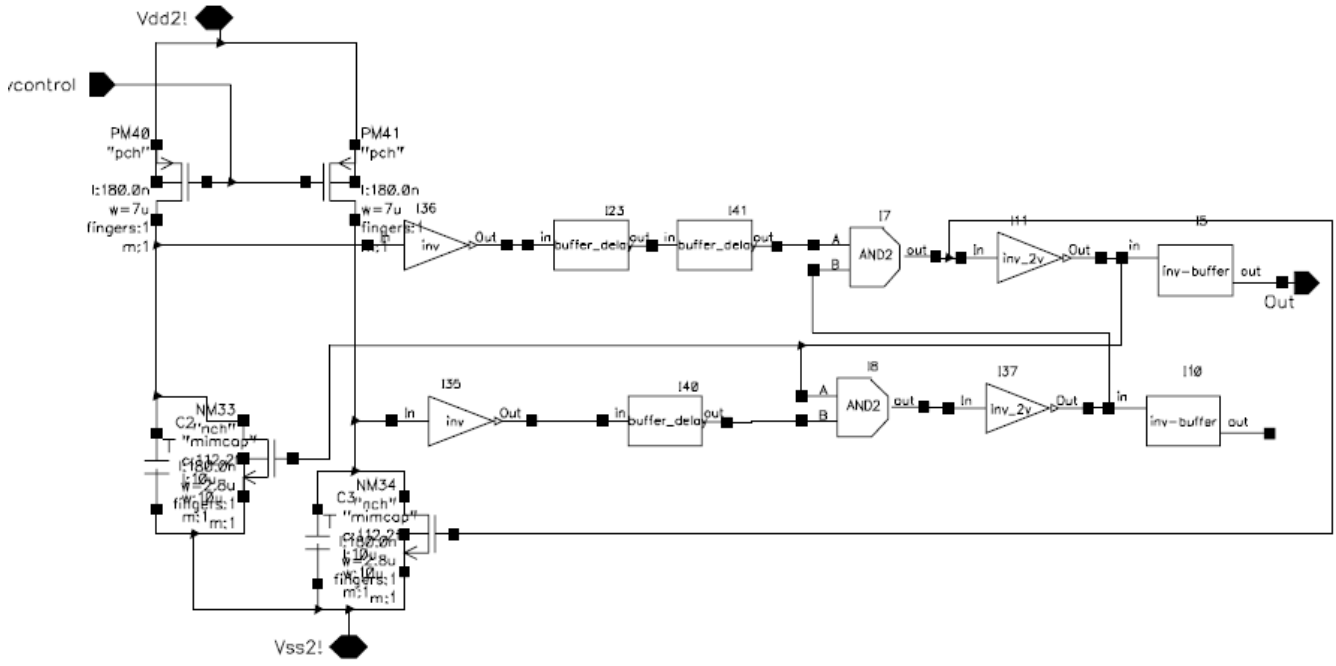

Figure 4.4 Schematic Circuit of Wide Range VCO with Center Frequency around 800 MHZ

As shown in Figure 4.4, two buffer delay blocks (I23 and I41) are added on the input to the first (top) NAND (AND+Inverter) gate and one buffer delay block is added on the input to the second (bottom) NAND (AND+Inverter) gate to slow down the oscillating speed. Also the gate voltage to N channel transistor (NM34) needed to have less delay to get close to 50% duty cycle pulse. This is accomplished by using the output of the first AND gate rather than the output of the second NAND (AND+Inverter) gate. The final block to the output is the inverter buffer to drive the loading and trim the oscillator output to be a good pulse shape as shown in Figure 4.5. Sizing has to be adjusted to drive the inv-buffer combination. Usually the center frequency is set at vcontrol equals VDD/2 to maximize the tuning range frequency by adjusting the control voltage. The wide range

VCO is a full switching saturated type ring oscillator where the high voltage is near VDD and low voltage is near zero. This type of ring oscillator gives better phase noise performance compared to one where the high and low voltages are not near the rails [103].

Figure 4.5 gives several schematic level simulation results with TSMC 0.18 um CMOS model under Cadence Analog Design Environment, which covers the DC control input from 0.65v to 1.2v.

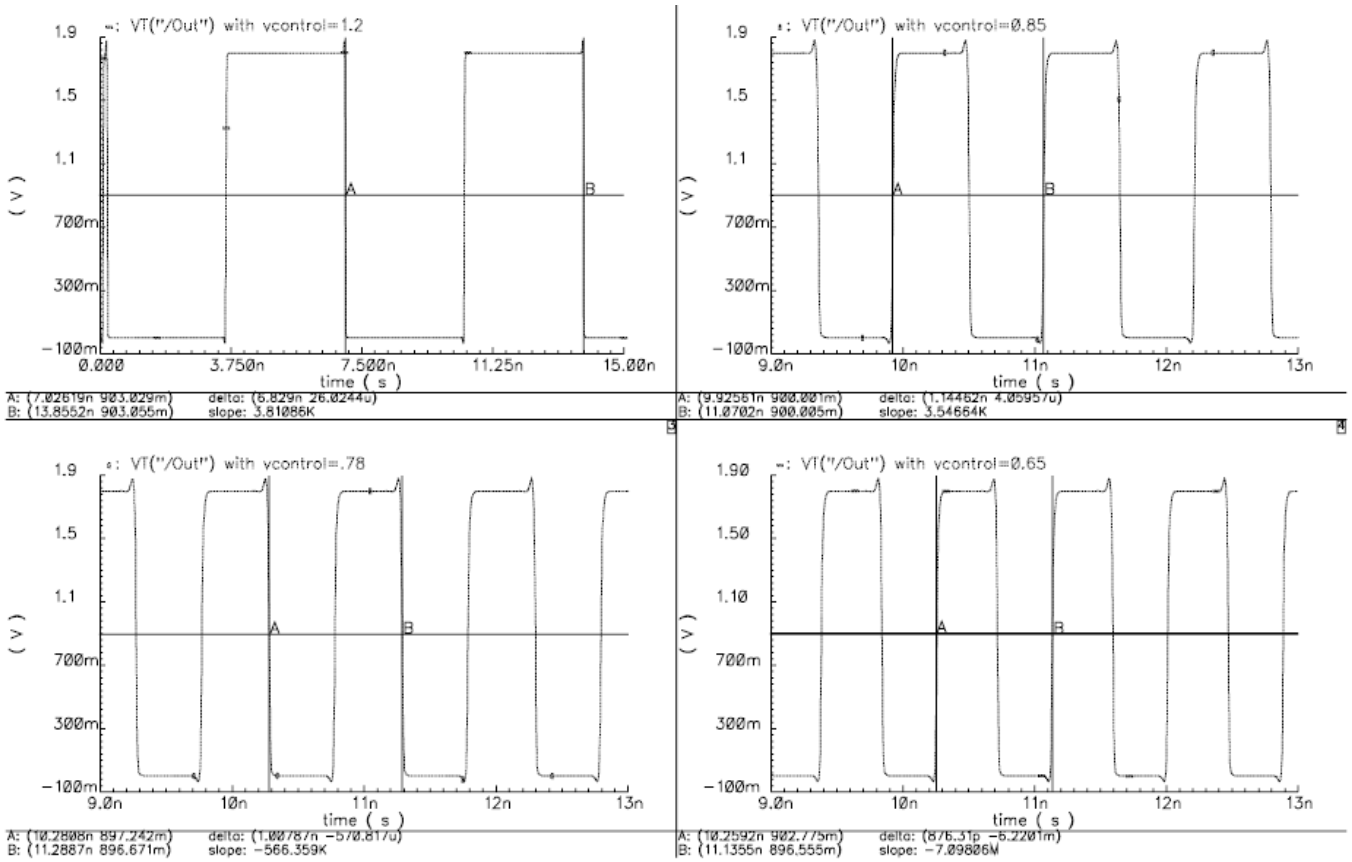

Figure 4.5 Schematic Simulation Results of Wide Range VCO

Top Left Figure: Output of the VCO with voltage control equals 1.2v

Top Right Figure: Output of the VCO with voltage control equals .85v

Bottom Left Figure: Output of the VCO with voltage control equals .78v

Bottom Right Figure: Output of the VCO with voltage control equals .65v

From Figure 4.5, it can be seen that all the four pulse signals are square waves with duty cycles close to 50%. Table 4.1 summaries more simulation results with variation of the DC control input (vcontrol).

Table 4.1 Wide Range VCO Tuning Range

vcontrol	frequency(GHz)	period(ns)
1.20	0.15	6.83
1.10	0.35	2.88
1.00	0.57	1.75
0.95	0.68	1.47
0.90	0.78	1.28
0.85	0.87	1.15
0.80	0.96	1.04
0.78	0.99	1.01
0.75	1.04	0.96
0.70	1.11	0.90
0.65	1.14	0.88
0.60	1.16	0.86

The VCO frequency as a function of the controlled voltage is graphed in Figure 4.6. As seen in Figure 4.6, the frequency can cover from 150MHz to 1.16 GHZ with vcontrol tuning; the frequency changes linearly following the vcontrol ranging from 0.7v to 1.1v. The linear frequency range is 150MHz to 1.1GHz with a center frequency of about 780MHz at vcontrol equal to 0.9v. This is close to the expected value of 800MHz.

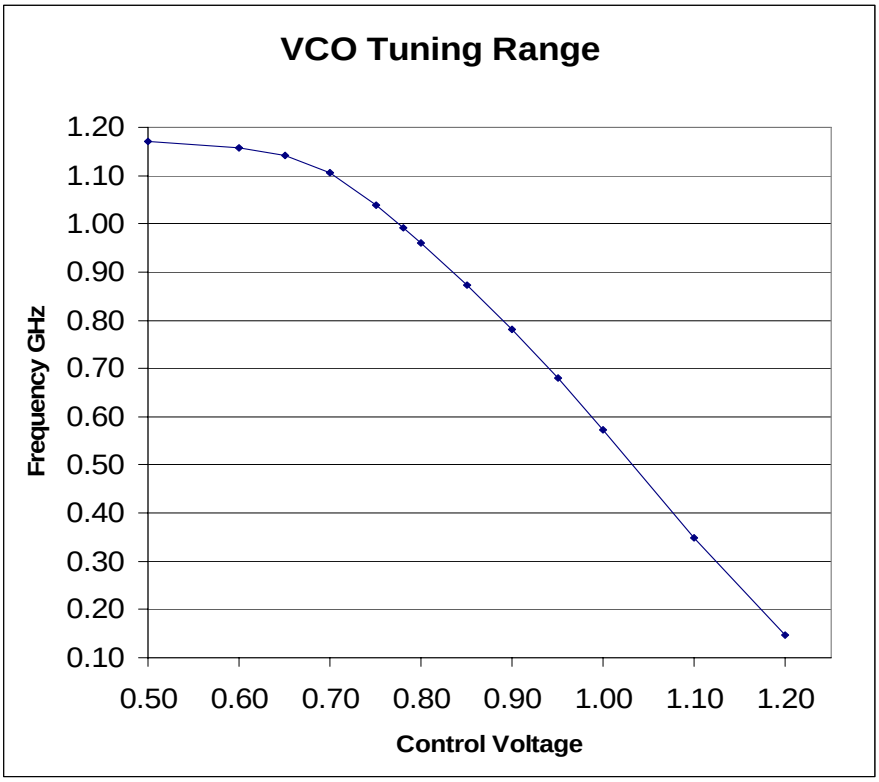

Figure 4.6 Wide Range VCO Tuning Range Centered at 780 MHz

The above discussed wide range VCO phase noise is executed by using Cadence Affirma RF Simulator (Spectre RF) Tool. The results are shown in Figure 4.7.

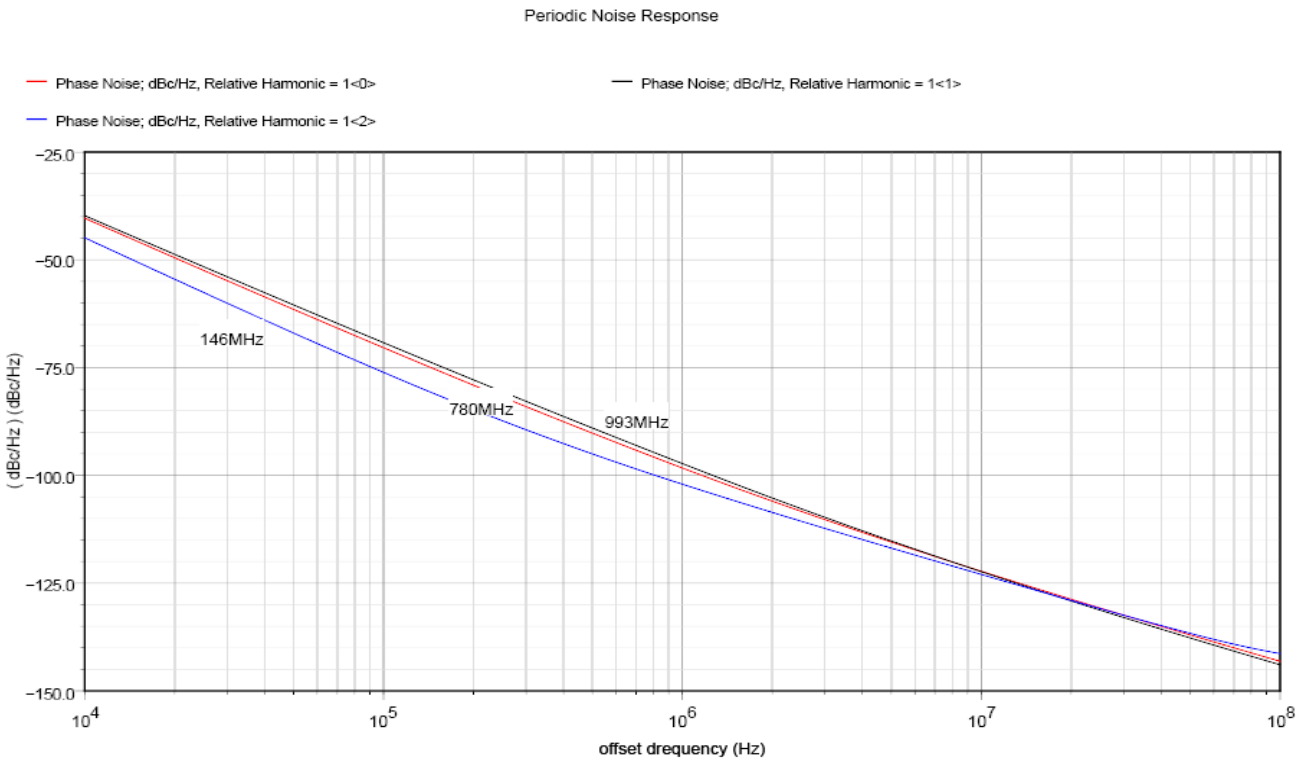

Figure 4.7 Simulated Phase Noise of Wide Range VCO with Center Frequency 800 MHz

Top Black Signal: Phase Noise at 993 MHz Carrier Frequency

Middle Red Signal: Phase Noise at 780 MHz Carrier Frequency

Bottom Blue Signal: Phase Noise at 146 MHz Carrier Frequency

From Figure 4.7, it can be seen the phase noise is -93 dBc/Hz at 1 MHz offset and -123 dBc/Hz at 10 MHz offset with 993 MHz carrier. The power consumption is 4.4 mW at 993MHz oscillating frequency.

Figure 4.8 shows the physical layout of the above discussed wide range VCO which has size of 60um by 42um. The large layout on the left side are the two capacitors. The right side of the layout comprises the gate components. It is noted that the wide range VCO will be much smaller if we can eliminate the capacitors which will be discussed below. This layout was fabricated as the clock generator for the PDSM ADC.

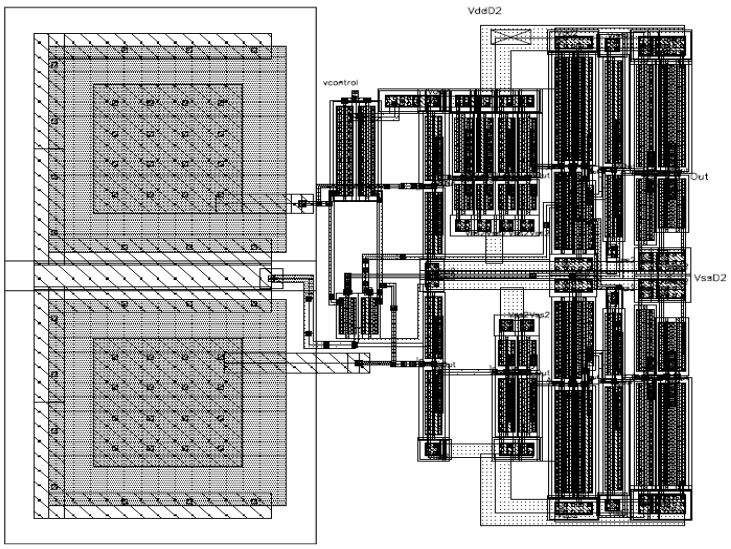

Figure 4.8 Physical Layout Of Wide Range VCO

To increase the oscillating frequency, one buffer is eliminated on each loop as shown in Figure 4.9. The tuning range is changed from the previous range of 136MHz to 1.16 GHz to a higher range of 360 MHz to 1.36 GHz as shown in Figure 4.10. The new linearity range is 360 MHz to 1.27 GHz compared to the previous design of 130 MHz to 1.1GHz. The center frequency is close to 900 MHz. The phase noise is shown in Figure 4.11. With 996 MHz carrier, the phase noise is -96 dBc/Hz at 1 MHz offset and -121 dBc/Hz at 10 MHz offset; the power consumption is 4 mW at 996 oscillating frequency. It can be seen that eliminating one buffer reduces the power consumption and increases the oscillating frequency. This is because the number of transistors and gate delay are both reduced. It is also observed that the phase noise has almost no change.

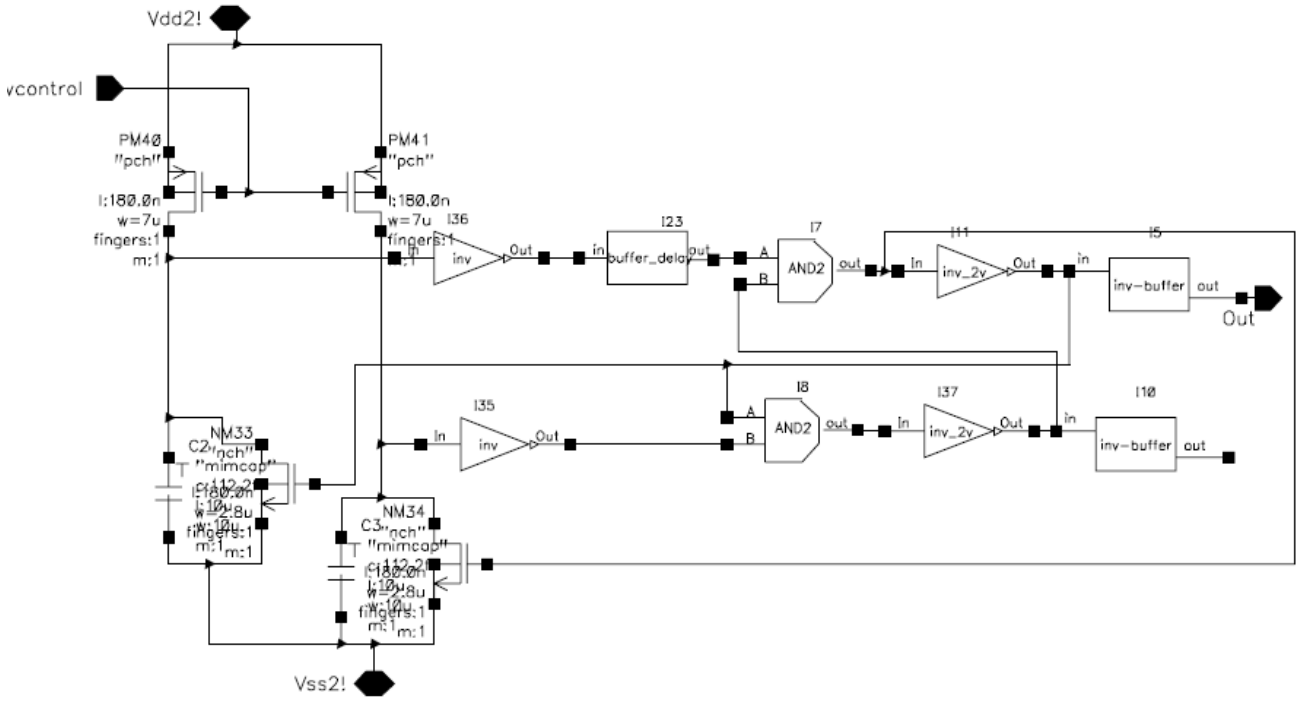

Figure 4.9 Schematic Circuit of Wide Range Voltage Controlled Oscillator with Center Frequency around 900 MHZ

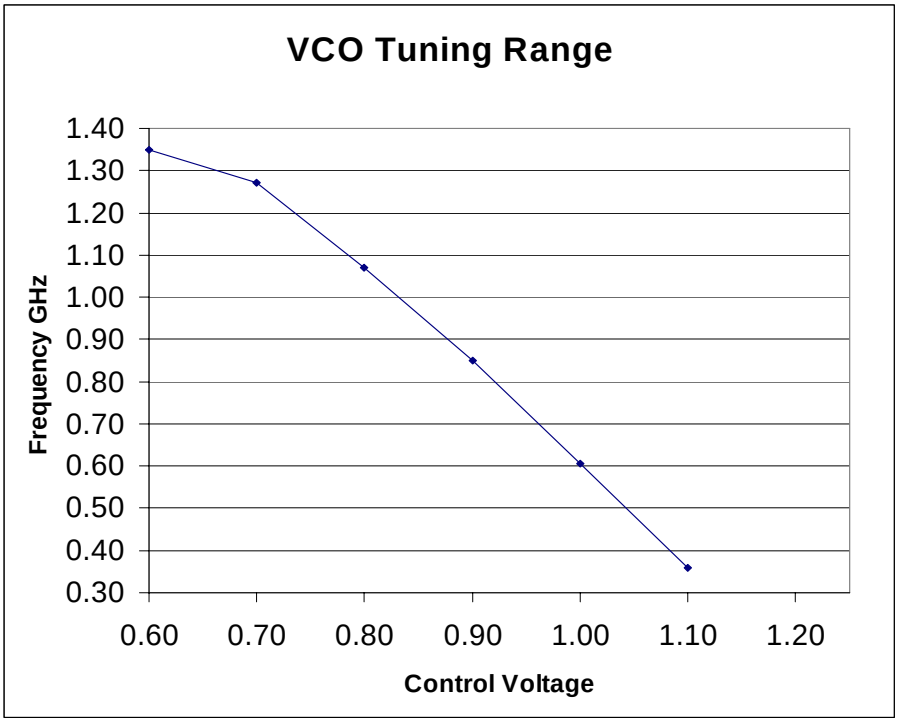

Figure 4.10 Wide Range VCO Tuning Range Centered at 900 MHz

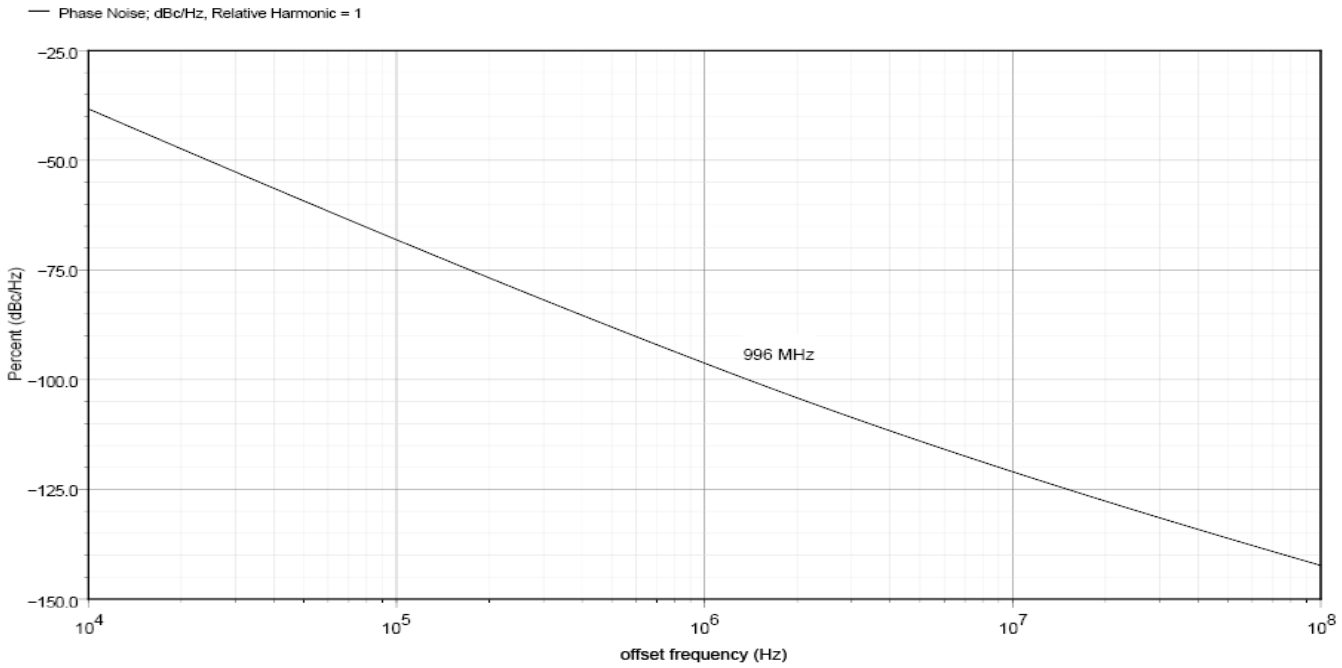

Figure 4.11 Simulated Phase Noise of Wide Range VCO with Carrier Frequency of 996 MHz

To increase the oscillating frequency more, the capacitors C0 and C1 are removed, so the total charging capacitor will be only Cds and Cgs as shown in Figure 4.12. The schematic simulation results show that the frequency tuning range is 400 MHz to 2.63 GHz and the linear frequency range is 400 MHz to 2.42 GHz as seen in Figure 4.13. The phase noise figure is shown in Figure 4.14. With 1.0 GHz carrier frequency, the phase noise is -92.5 dBc/Hz at 1 MHz offset and -113.8 dBc/Hz at 10 MHz offset. The power dissipation is reduced to 3.0 mW at 1 GHz oscillating frequency due to the reduced node capacitance (dynamic power $\propto C_{TOTAL}*V_{dd}^2*f_{osc}$).

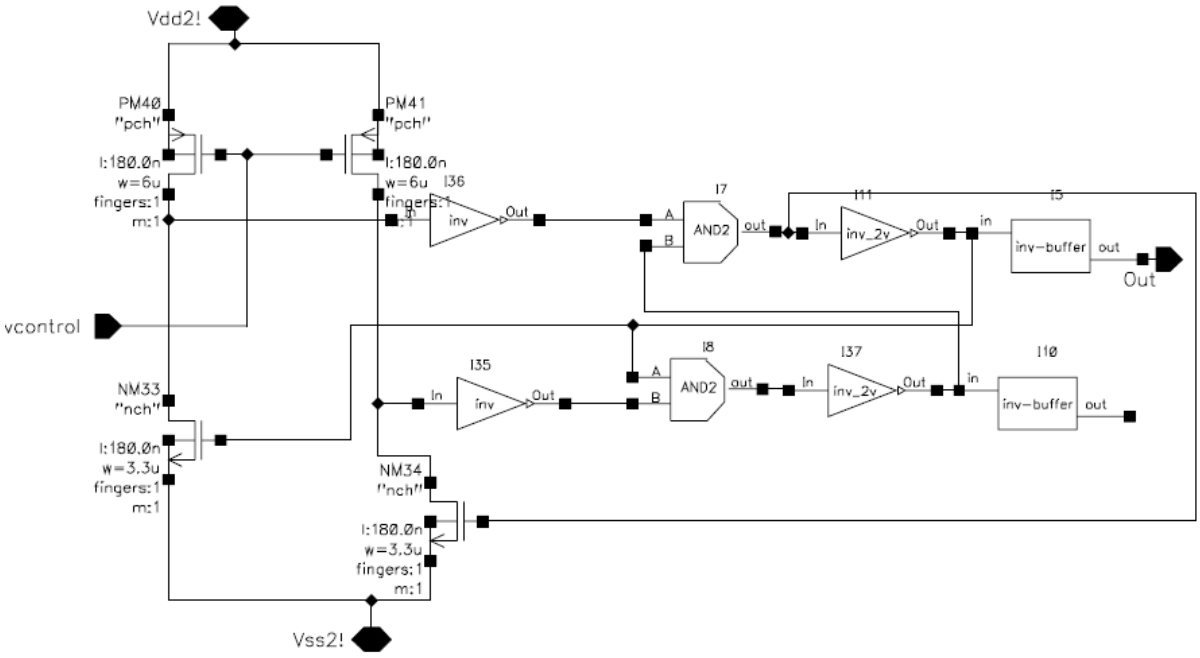

Figure 4.12 Schematic Circuit of Wide Range Voltage Controlled Oscillator with Center Frequency around 1.6 GHZ

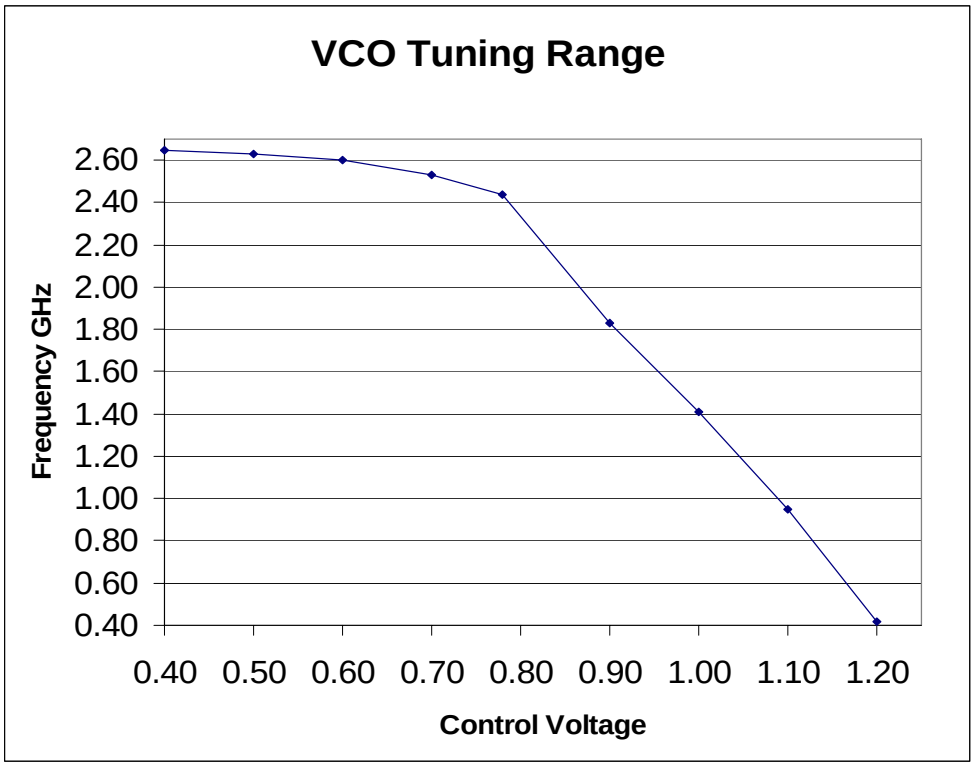

Figure 4.13 Wide Range VCO Tuning Range Centered at 1.6 GHz

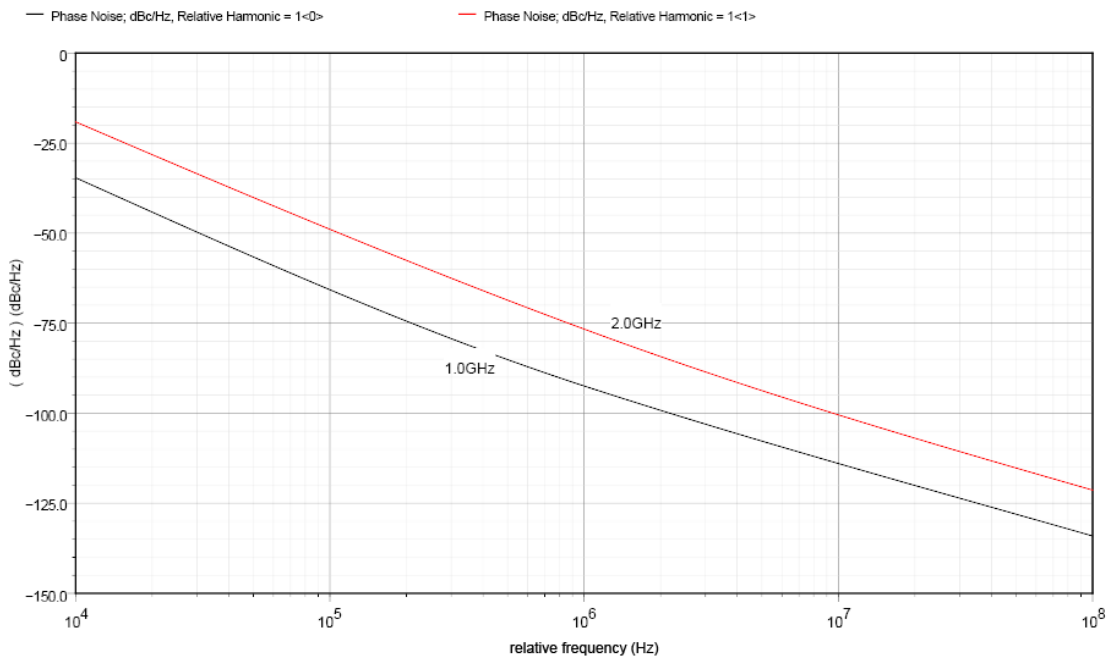

Figure 4.14 Simulated Phase Noise of Wide Range VCO with Center Frequency 1.6 GHz

Using the above discussed principle of increasing the oscillating frequency, Figure 4.15 demonstrates a wide range VCO schematic circuit which can reach as high as 4.1 GHz oscillating frequency. It can be seen that the AND gates are replaced by NAND gates to save one inverter gate delay and also the current source transistor sizes are increased to enhance the source current. The unbalanced gate delay of top and bottom is compensated by using smaller size of NM34 than NM33. The smaller of the transistor is, the less of the parasitic capacitances Cdb and Cgs are, and then also reduces the charging time. Each gate's size is adjusted to keep the minimum delay and also be able to drive the loading.

Figure 4.16 shows the tuning range which is 879 MHz to 4.1 GHz. The linear range is about 1.0 GHz to 3.4 GHz. The phase noise is shown in Figure 4.17. As seen the phase noise is -95.4 dBc/Hz at 1MHz offset and -114.6 dBc/Hz at 10 MHz offset with 2.0 GHz

carrier frequency. The power dissipation is 3.1 mW with 1.0 GHz oscillating frequency. And the physical layout is 18um by 38um which is smaller than the low frequency VCO.

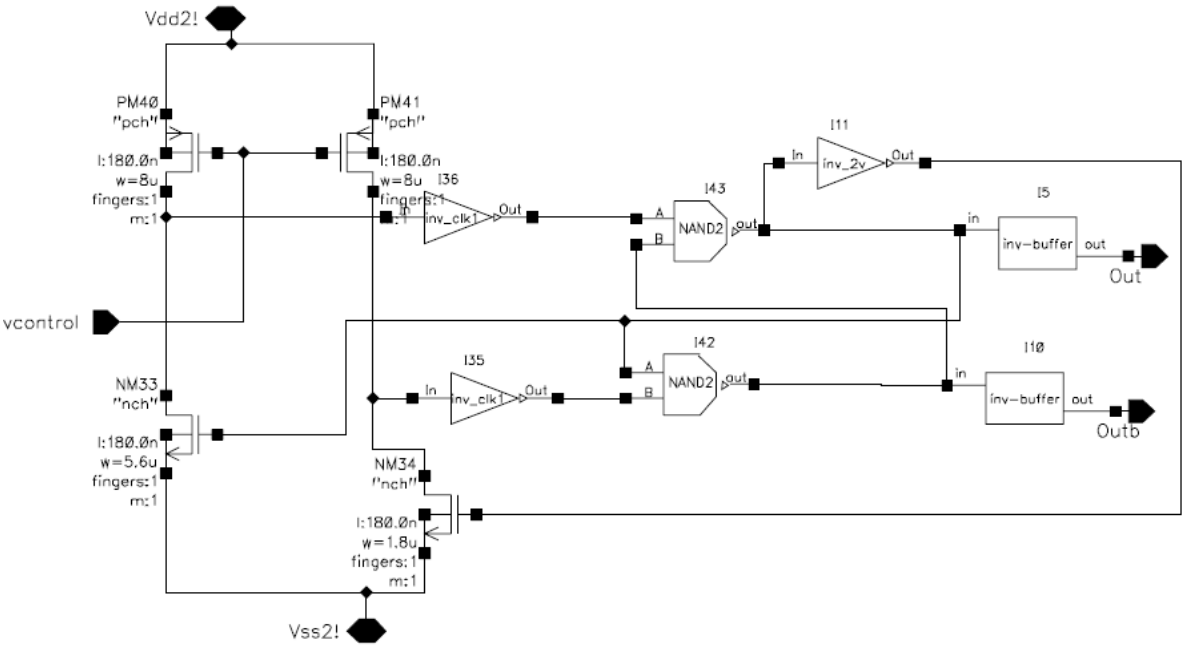

Figure 4.15 Wide Range VCO Schematic Circuit with Center Frequency 2.0 GHz

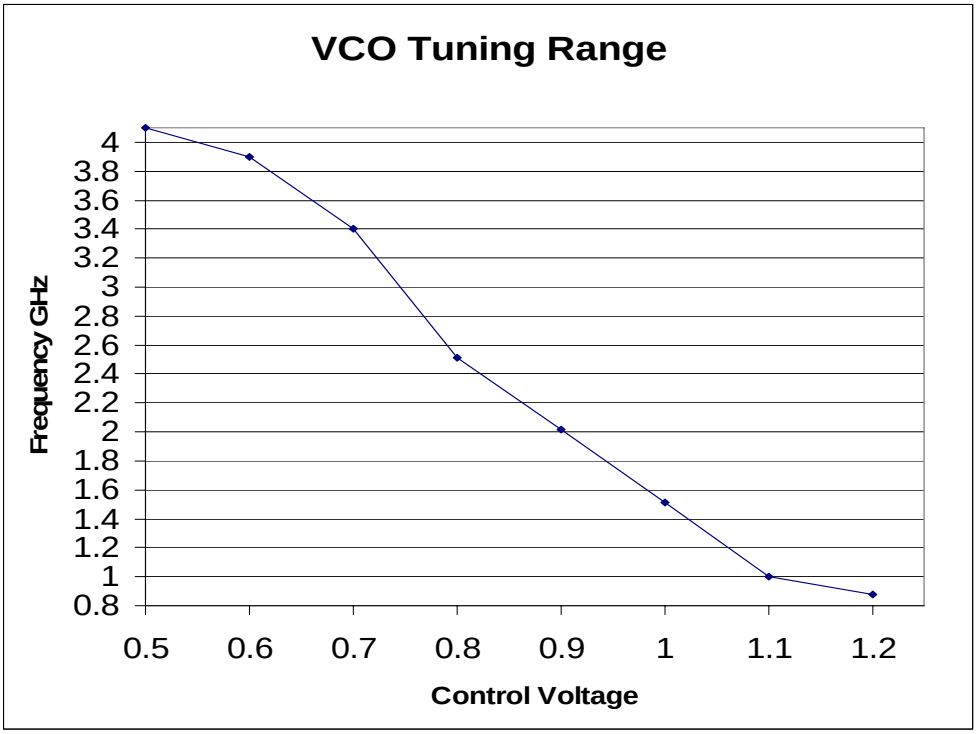

Figure 4.16 Wide Range VCO Tuning Range Centered at 2.0 GHz

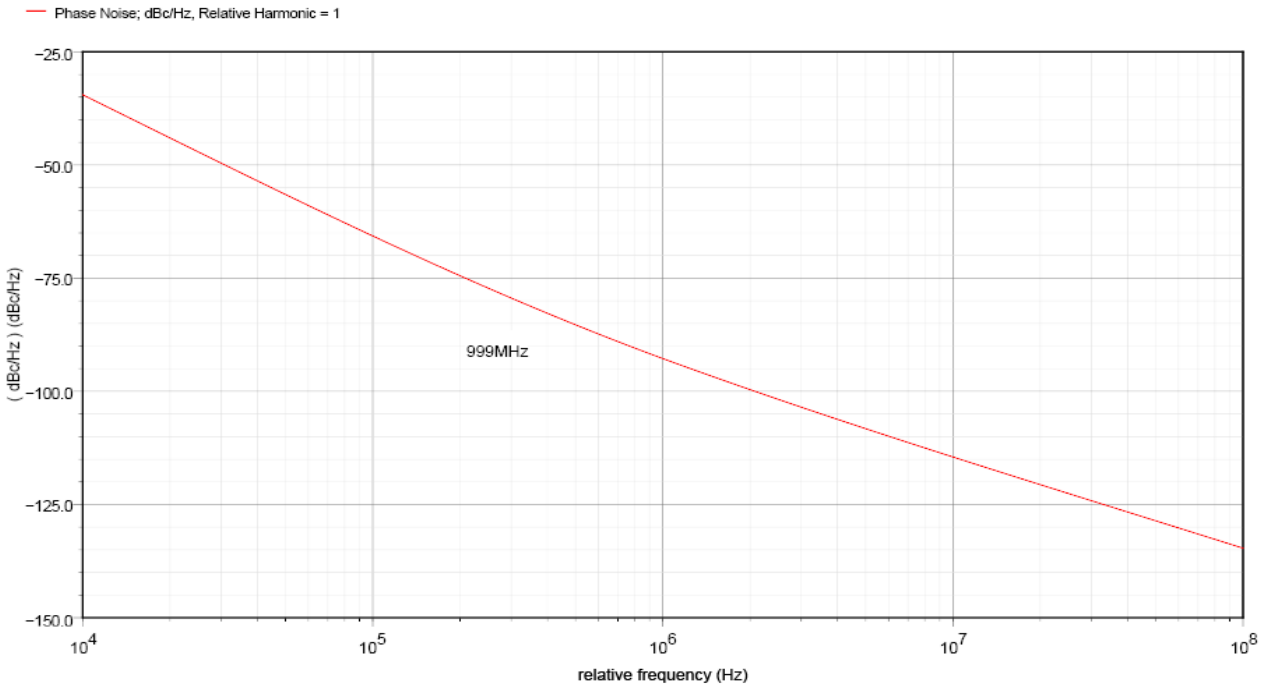

Figure 4.17 Simulated Phase Noise of Wide Range VCO with Center Frequency 2.0 GHz

The overall wide range VCO performances are summarized in Table 4.2. It can be seen the wide range VCO frequency has great flexibility in choosing an operating frequency, which can go as high as 4.1 GHz with 180nm CMOS technology and as low as 150MHz.

Table 4.2 Wide Range VCO performances

Schematic Figure	Tuning Range (GHz)	Linear Range (GHz)	Center Frequency (GHz)	Power Dissipation at 1.0GHz (mW)	Phase Noise (dBc/Hz)	
					at 1MHz	at 10MHz
4.4	.15~1.16	.15~1.1	0.8	4.4	-93	-123
4.9	.36~1.36	.36~1.27	0.9	4.0	-96	-121
4.12	.4~2.63	.4~2.42	1.6	3.0	-92.5	-113.8
4.15	.879~4.1	1.0~3.4	2.0	3.1	-93	-114

4.2.3 Measurement Results for Center Frequency at 800 MHz

The wide range VCO with center frequency 800 MHz was integrated on chip as the ADC clock source. Figure 4.18 gives the block diagram of the on chip clock source on ADC application. The on chip block diagram gives the option of using on chip VCO or external clock which can be selected by a two inputs multiplexer which is composed of two switches. The on chip clock is generated by clk-vc-wide-2v block which is centered at 800 MHz. Vcontrol is the voltage control signal for the on chip VCO. If the multiplexer control signal cs1 is set to low "0", the on chip clock signal goes to the clkout; if cs1 is set to high "1", the external clock is getting through the switch to clkout. This clkout signal will be used for the entire ADC system clock source which includes driving all the clock tree network. The on chip clock custom layout is shown in Figure 4.19 which was fabricated as part of the ADC IC. The range of the on chip voltage controlled ring oscillator clock was tested by measuring a decimated clock signal that is available off chip via an output buffer. The tested results show the on chip clock frequencies varies from 4.0 MHz to 1.0 GHz with an external voltage controlled input that varies from 0.6 volts to 1.35 volts. Figure 4.20 and Figure 4.21 demonstrate the output of the decimated clock after dividing by 8, so that 1.0 GHz on chip clock corresponds to a decimated off chip signal of 125 MHz and 4.0 MHz corresponds to 500 KHz. The decimated clock and decimated ADC digital outputs are compatible with a Logic Analyzer which can only reach a clock frequency of 200MHz for synchronization measurement.

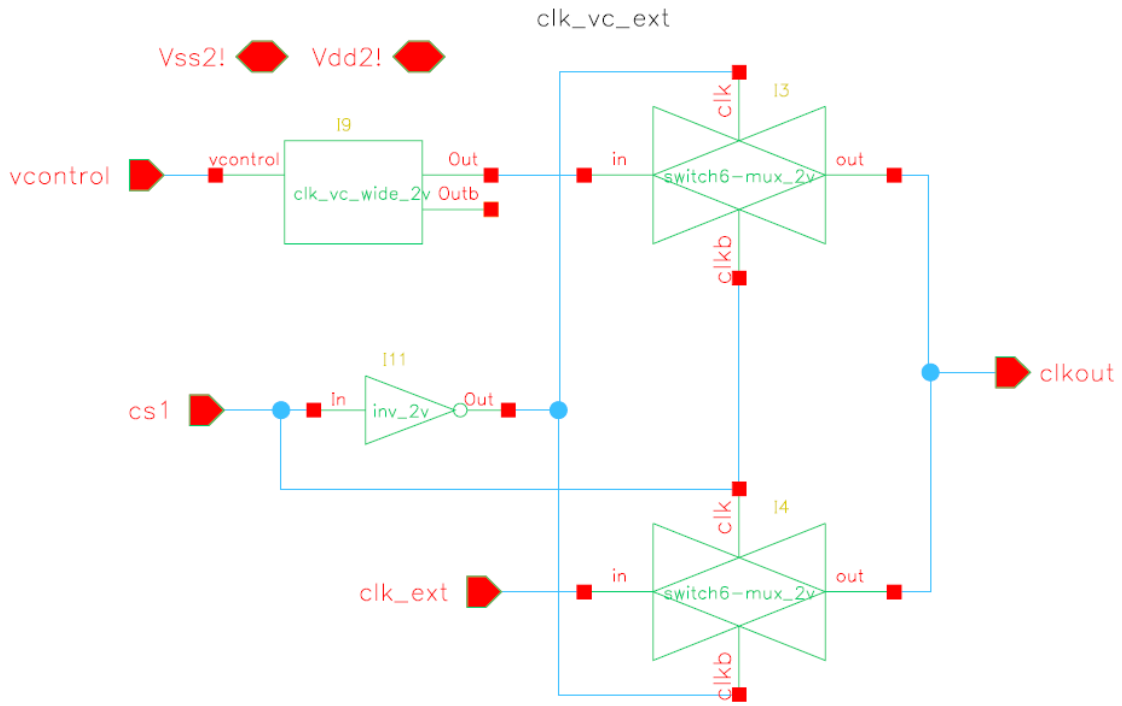

Figure 4.18 On Chip Clock Block Diagram Centered at 800 MHz

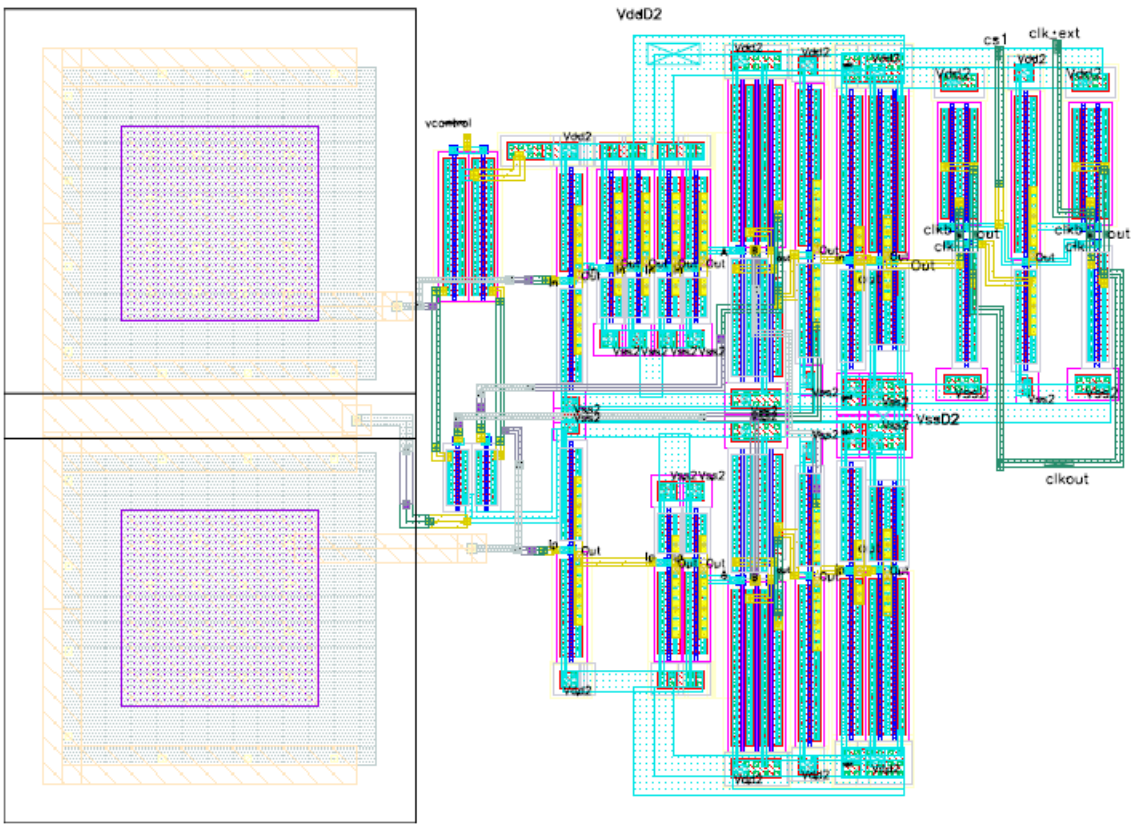

Figure 4.19 On Chip Clock Physical Layout Centered at 800 MHz

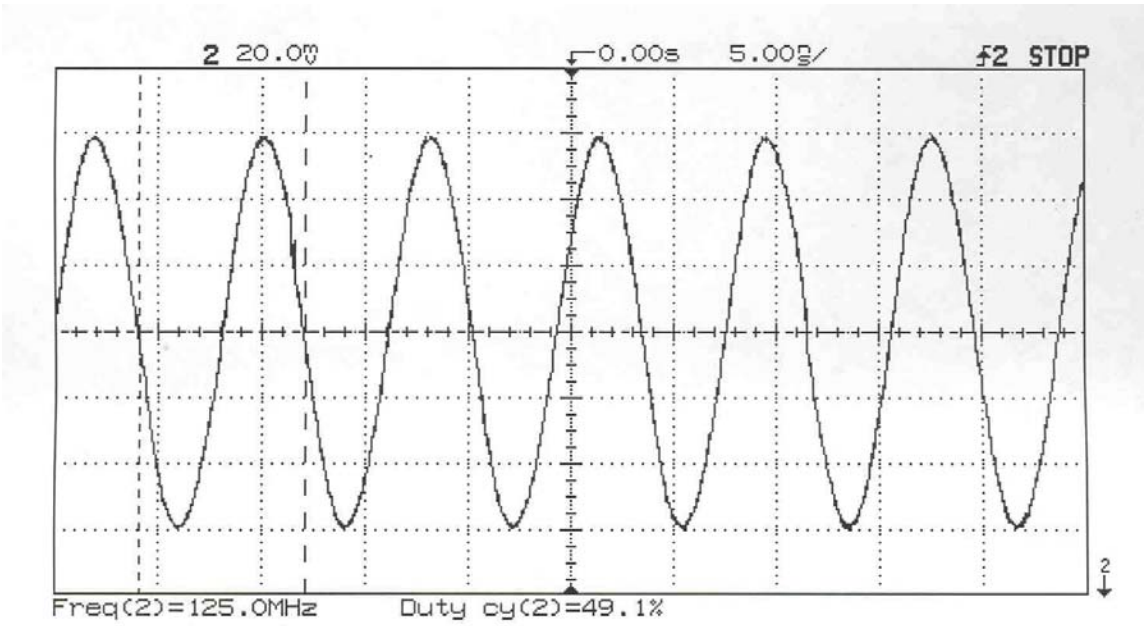

Figure 4.20 Decimated off Chip Clock Output of 125 MHz (corresponds to 1 GHz on chip clock)

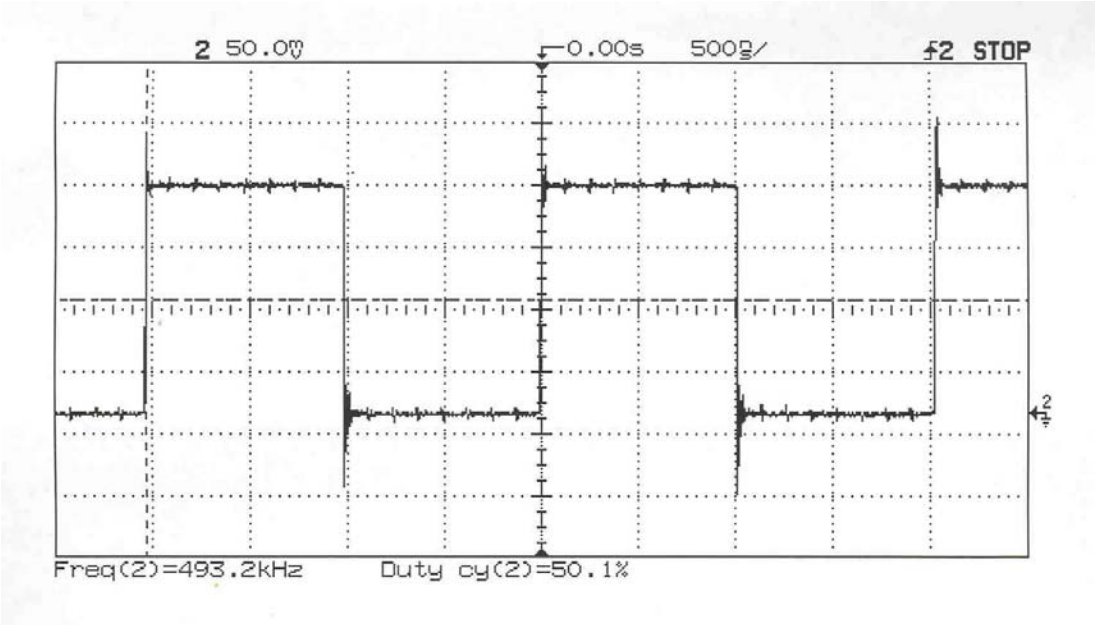

Figure 4.21 Decimated off Chip Clock Output of 500 KHz (corresponds to 4 MHz on chip clock)

As shown in Figure 4.21, the lower frequency clock has a square wave output. This is because the on chip digital output buffer can charge and discharge the Oscilloscope 13pF

input load easily at the 500KHz frequency. As the clock frequency increases, the charging and discharging time are apparent and the decimated clock output does not reach 1.8 volts nor 0 volts for high and low. This is seen in Figure 4.20 for the 125 MHz decimated clock.

4.3 I/Q Voltage Control Oscillator Design

4.3.1 Four Stage Ring Oscillator with Dual Delay Paths

The dual delay VCO [104,105] concept is adopted to increase the oscillating frequency and tuning range compared to the conventional ring oscillator. The differential fully switching delay cell is used to reduce the phase noise of the ring oscillator and then to get stable clock source. The basic dual delay VCO architecture uses four differential delay cells in a loop as shown in Figure 4.23. Each cell as shown in Figure 4.22 has a differential structure to reduce the power supply injected phase noise.

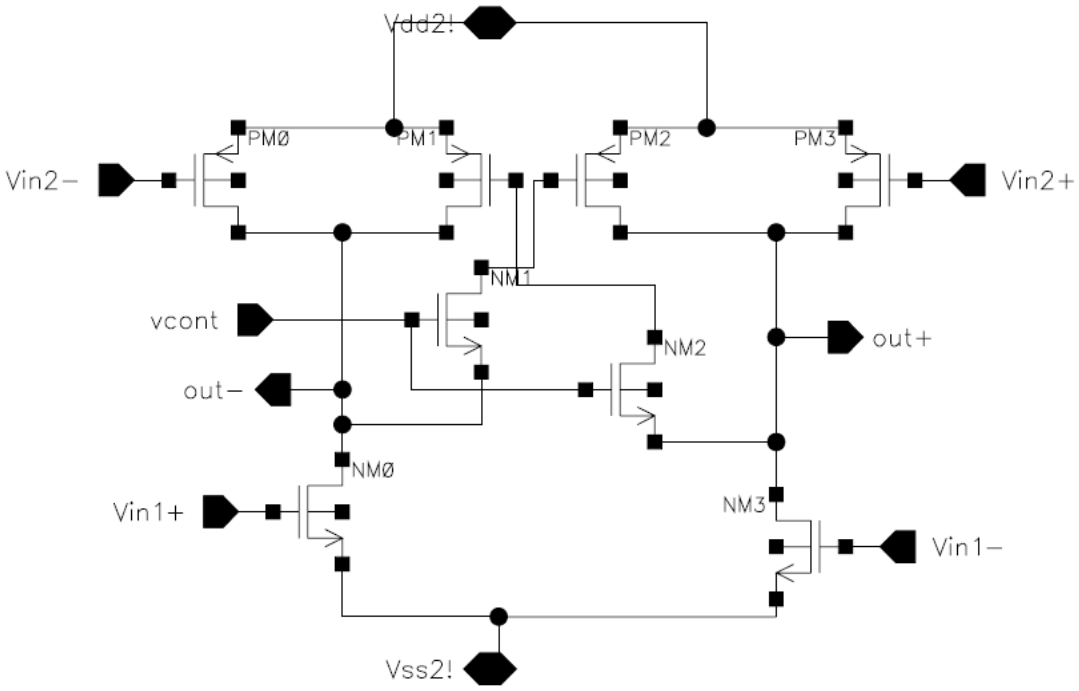

Figure 4.22 4 Input Differential Delay Cell

As seen in Figure 4.22, the architecture is essential a differential ring oscillator with dual delay paths. The loading PMOS transistors PM1 and PM2 are added to build a CMOS latch. The cross coupled NMOS transistors NM1 and NM2 are used to control the maximum gate voltage of the PMOS loading transistors and limit the strength of the added latch. The control voltage vcont control the output driving current of the PMOS load and the delay time. When vcont drops, the channel resistance of NM1 and NM2 are increased and the latch strength is weaker, so switching the state is easier and results in less delay and higher oscillating frequency. Otherwise, the oscillating frequency will go to lower. A full swing waveform is generated from the essential differential inverter, which enables the VCO to drive digital circuitry. The dual delay scheme is implemented by using both a negative skewed delay path and a normal delay path in the same ring oscillator. As shown in Figure 4.22, PM0 and PM3 are added to take the negative skewed signal (Vin2+, Vin2-). The normal signal is connected to the NMOS inputs (Vin1+, Vin1-). As seen in Figure 4.23, the negative skewed signal is taken from the output of two stages before the current delay stage. This helps the PMOS to prematurely turn on during the output transition and compensates for the PMOS slower mobility compared to NMOS, so to reduce the transition time.

Overall, the dual delay VCO reduces the phase noise and also the rising time and falling time of the output compared to the conventional ring VCO. Based on these features, the dual delay VCO is fully investigated by using both TSMC 0.18um and IBM 0.18um CMOS techniques.

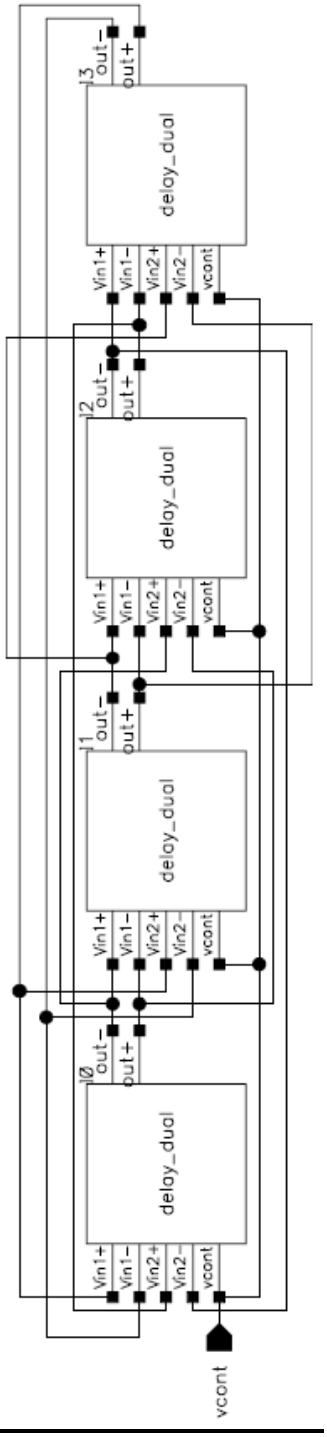

Figure 4.23 VCO with Dual Delay Path

A four stage dual delay VCO is designed and fabricated through IBM 0.18um CMOS process. The top level schematic circuit is shown in Figure 4.24, which has four in phase and quadruture outputs.

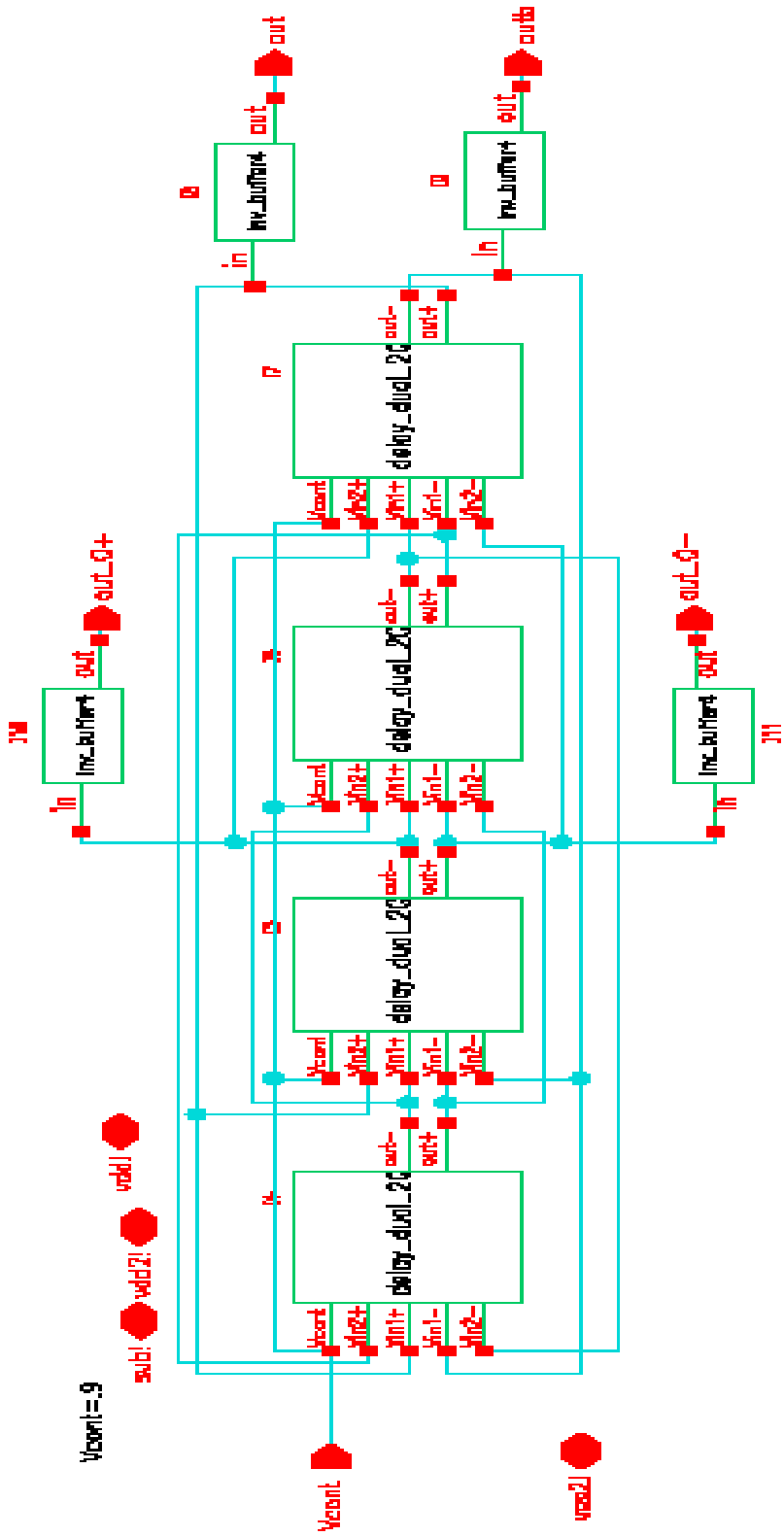

Figure 4.24 Four Stage Ring Oscillator with Dual Delay Paths

Figure 4.25 shows the gain of the VCO is equal to 2.0 GHz/v; the linear tuning range is 1.83 GHz to 2.13 GHz; the center frequency is 2.0 GHz at the voltage control input of 0.9v. As seen from Figure 4.25, the oscillating frequency reduces while increasing the DC control voltage, which matches the above discussion.

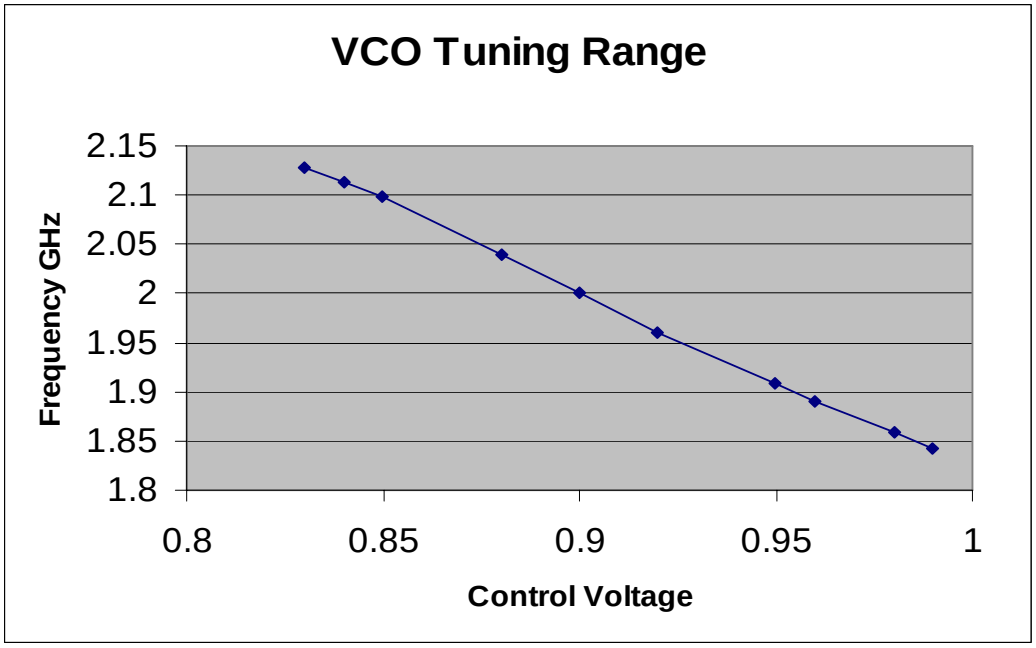

Figure 4.25 Dual Delay VCO Tuning Range

The dual delay VCO has been captured by Cadence Virtuso Composer Schematic tool with IBM 0.18um process. The schematic transient simulation results are shown in Figure 4.26 and Figure 4.27. From Figure 4.26, it can be seen that output signals "out" and "outQuad" are 90 degrees phase shifted. Figure 4.27 shows signals "out" and "outb" are 180 degrees phase shifted. The fourth output "outQuadb" is not shown in the plot figures, which is the differential output of "outQuad".

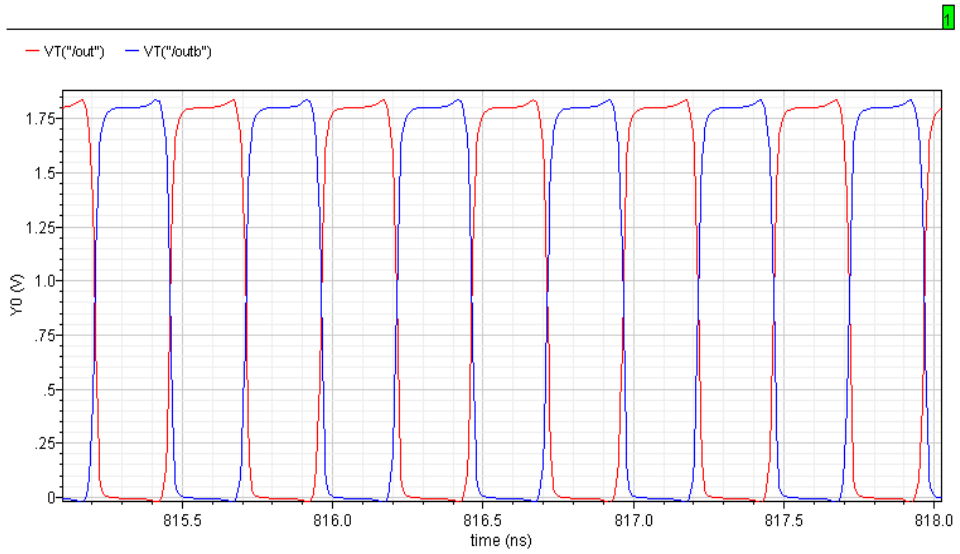

Figure 4.26 Dual Delay I/Q VCO out and outb

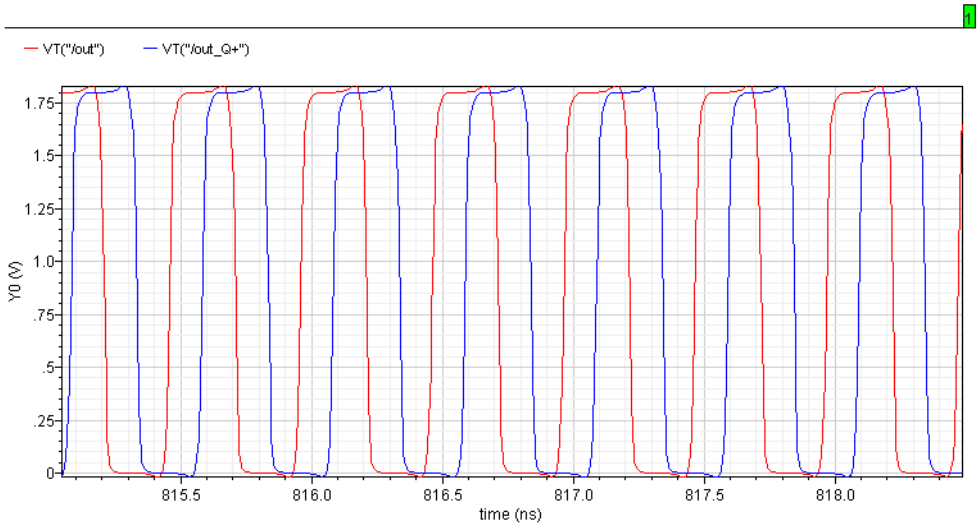

Figure 4.27 Dual Delay I/Q VCO out and outQuad

The FFT was done by using Cadence FFT special function. The result is shown in Figure 4.28. The FFT accuracy is limited by workstation memory constraints. The phase noises are -88.0 dBc/Hz at 1 MHz offset and -118 dBc/Hz at 10 MHz offset with 2.0 GHz carrier frequency as shown in Figure 4.29. The average power consumption based on schematic simulations of the Dual Delay VCO was 8.1 milliwatts at 2 GHz oscillating frequency.

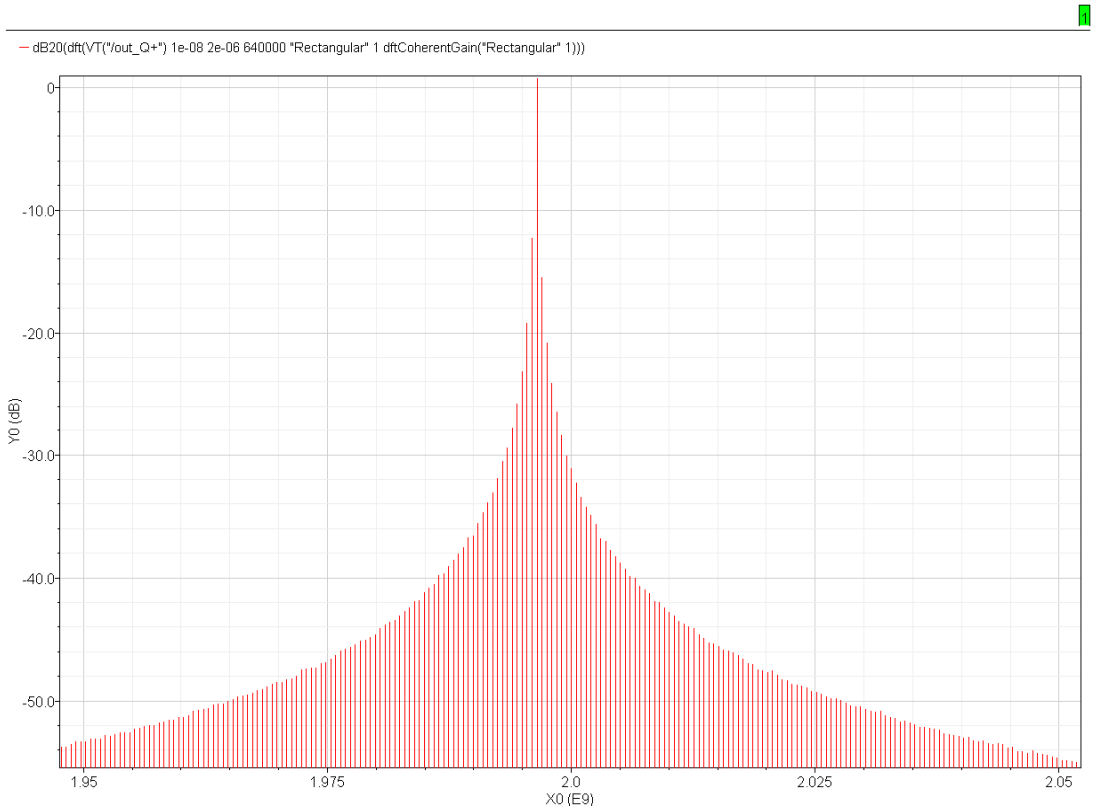

Figure 4.28 FFT Result of Dual Delay VCO

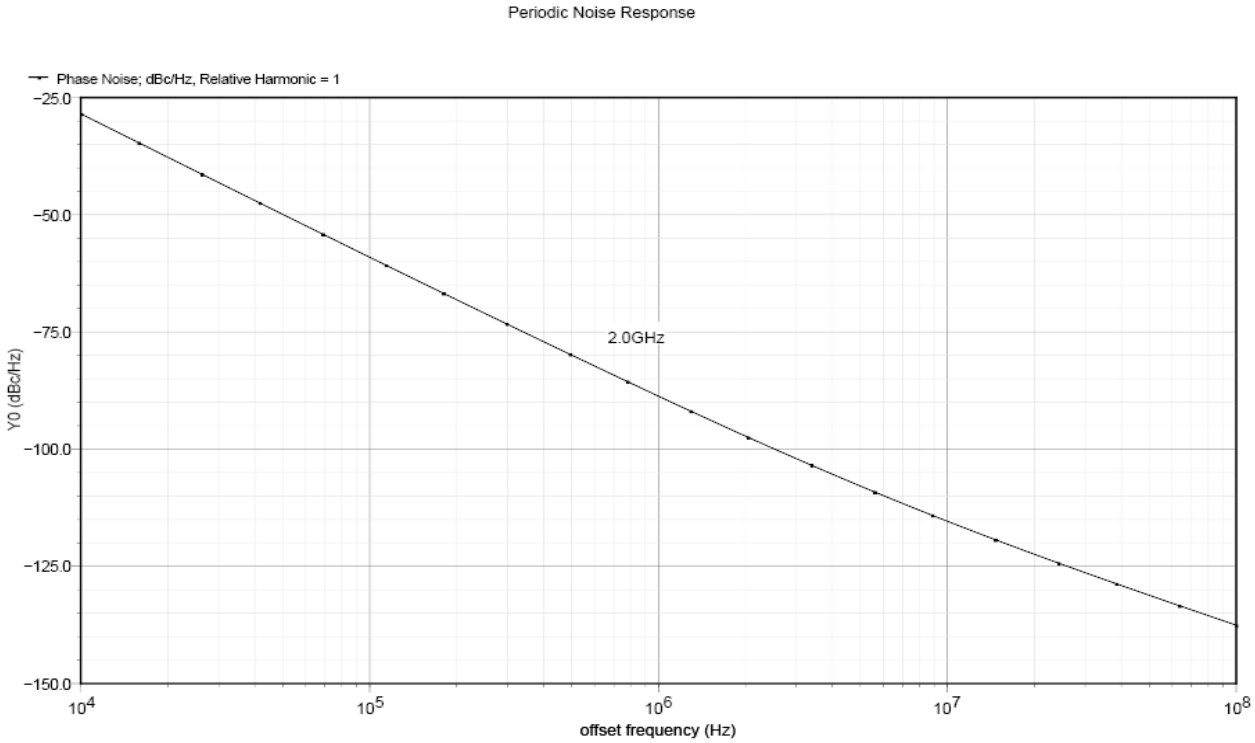

Figure 4.29 Simulated Phase Noise of Dual Delay VCO with centered frequency 2.0 GHz

4.4 Frequency Synthesizer

A frequency synthesizer is an electronic system for generating a range of frequencies from a single fixed time base or oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems [106]. The frequency synthesizer in wireless communication systems is usually implemented by a Phase-Locked Loop (PLL).

4.4.1 Phase Lock Loop with In Phase/Quadrature Design

PLLs are also the most popular types of clock generators which can lock the clock phase precisely referenced to the low frequency reference clock. Figure 4.30 shows the block diagram of PLL frequency synthesizer, which includes the Phase Frequency Detector (PFD), Charge Pump/Low Pass Filter (Loop Filter), VCO and clock divider.

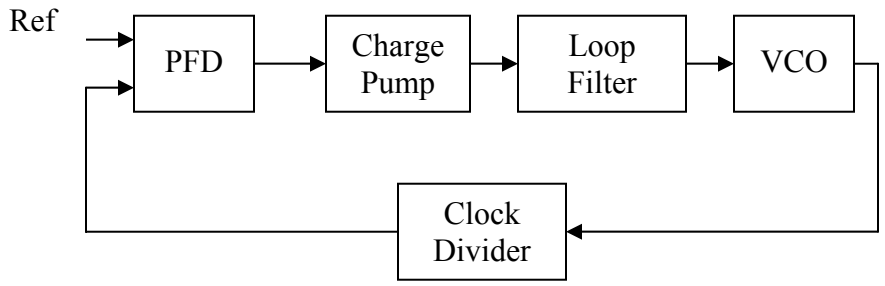

Figure 4.30 Block Diagram of PLL

The phase frequency detector is used to detect the phase difference between the low phase noise reference frequency and the decimated VCO frequency. The outputs of the PFD which are proportional to the phase difference will go to the charge pump to generate an analog voltage signal. The analog output signal of the charge pump is filtered, which is then the voltage control input for the VCO. The PLL uses a negative

feedback loop to bring the VCO frequency and phase in alignment with the input reference clock. Whenever the VCO and reference frequency phases are close enough that the PFD can't detect the difference, the output signal will be locked at that frequency and phase. To keep the locked frequency, it generally needs to have zero phase error in the lock which requires the control voltage to the VCO have a zero output from the phase detector (and hence zero phase error).

4.4.1.1 Detailed design of 2 GHz PLL with In phase and Quadrature output

A PLL with I/Q dual delay VCO has been designed by using IBM 0.18um technology as shown in Figure 4.31 which includes a Phase Frequency Detector (PFD), a Charge Pump/Low Pass filter, an In phase/Quadrature VCO and a Divider. The dual delay VCO architecture of Figure 4.24 is used in this PLL.

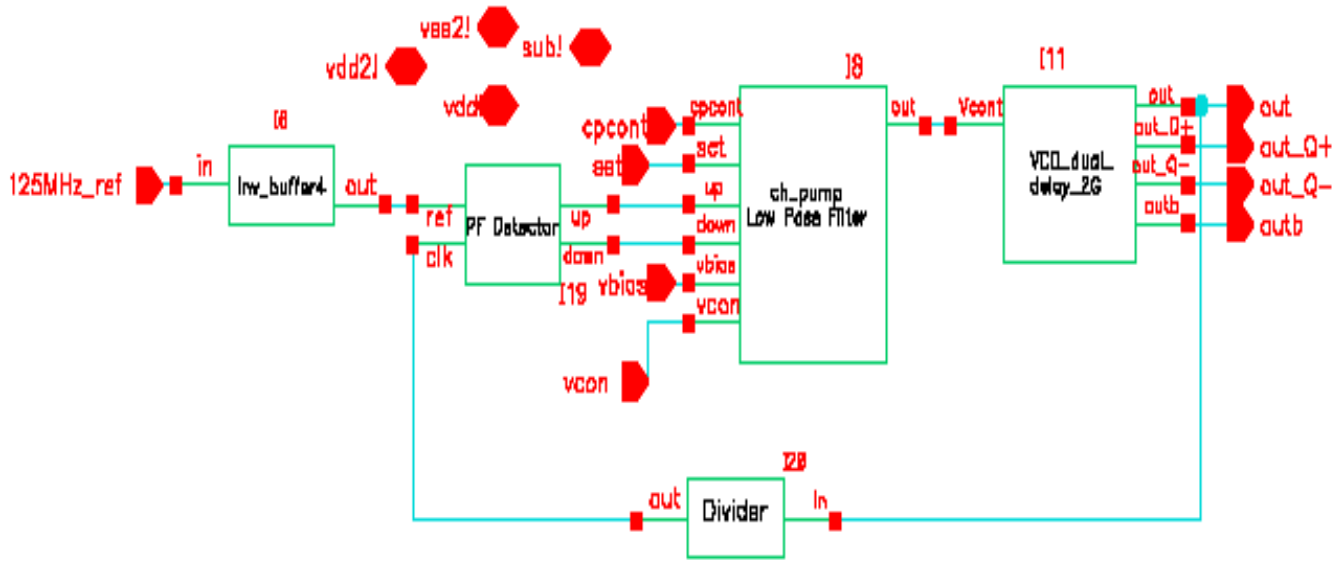

Figure 4.31 2GHz I/Q Dual Delay PLL

The following sections will give some detail discussion of each block in Figure 4.31.

4.4.1.1.1 Phase Frequency Detector (PFD)

The Phase Frequency Detector (PFD) circuit is implemented from standard logic elements as shown in Figure 4.32 [107], which has two input signals (ref and clk) and two output signals ("up" and "down"). The feedback signal (clk) rising edge is compared with the reference signal (ref) rising edge; when the reference clock "ref" is ahead of the feedback VCO clock signal "clk", the output signal "up" would generate a pulse and "down" keeps constant '0'; when the reference clock "ref" is behind of the feedback VCO clock signal "clk", the output signal "down" would generate a pulse and "up" keeps constant '0'. The width of the pulse is proportional to the time difference of the two inputs as shown in Figure 4.33. A detailed implementation example can be found in reference [108]. The key requirement for detecting the small phase difference of the two input signals is to keep the ref and clk signal paths precisely matching.

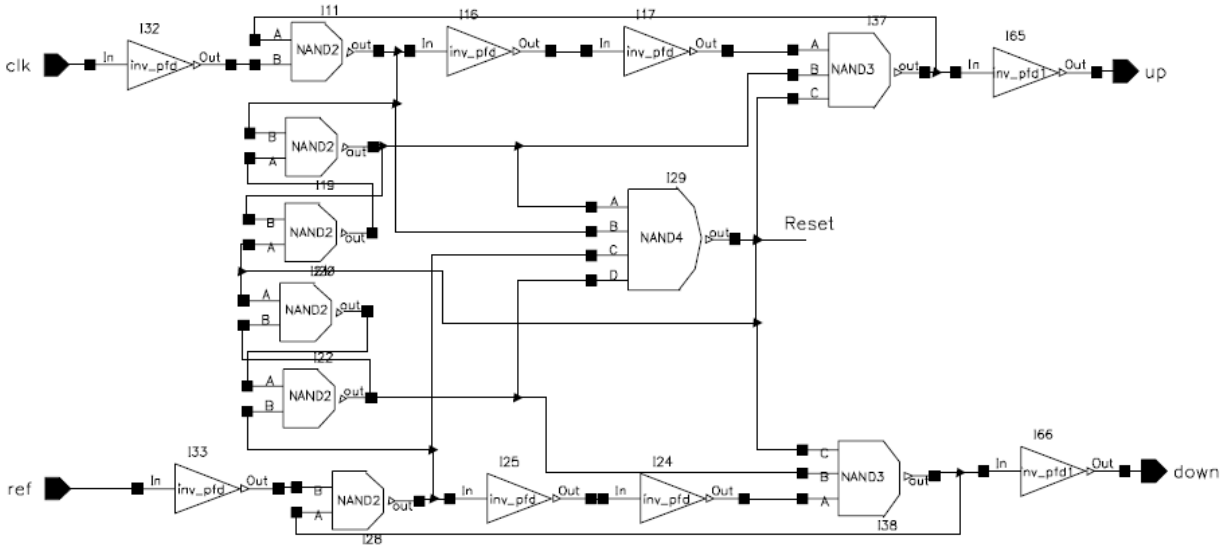

Figure 4.32 Phase Frequency Detector

As seen in Figure 4.32, the used standard NAND gates have different time delays from different inputs to output, for example 2-inputs NAND gates which has A and B two

inputs, the time delays from A to out and B to out are slightly different. For most digital applications, this delay difference can be ignored, but for the PFD, this will cause unbalance delays between the two paths and unequal response of detecting the phase difference of the two signals, and finally generate different pulse widths for "up" and "down" signals even for the same phase difference, which will result in the charge pump and loop filter output be biased in one direction. Then the output signal will be frequently modulated causing short term deterministic variations (jitter per phase noise) in the PLL output [109]. So to make sure the circuit response as fast as possible and with symmetry for both "up" and "down", the most important effort for this PFD architecture is to keep the two paths totally symmetrical. This requires the two paths have the same components and same pin connection to the same gate symbol as shown in Figure 4.32. A second important effort is to optimize each component's sizes to keep enough driving capability and minimum parasitic capacitance. Also the NAND3 and NAND4 gates are the longest delay components in Figure 4.32. Their delay affect the PFD detector response speed, so modifying these two gates architecture to obtain a high design is necessary. Following the above discussion effort, the Cadence simulation results for the PFD show that both "up" and "down" signals can respond to a 15 ps time difference for this 2GHz dual delay PLL design. As seen in Figure 4.33, the top signal is the 125MHz reference clock input; the second top signal is the divided by 16 VCO clock; the third top signal is the PFD output signal "up" and the bottom one is the PFD output signal "down". Several different input reference frequency phases have been simulated. The simulation results indicate the designed PFD is able to detecting 15ps time difference.

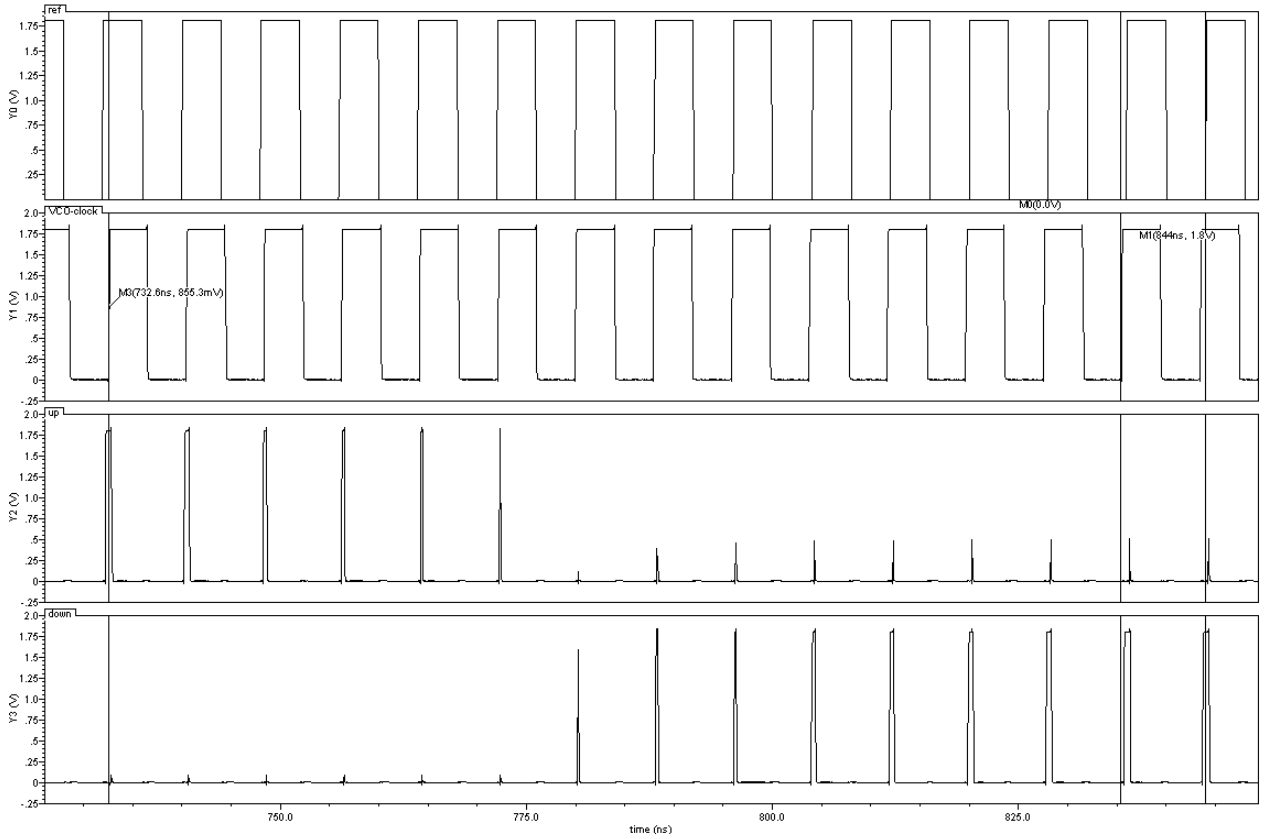

Figure 4.33 Schematic Simulation Results of PFD

Top signal: 125MHz reference clock input
Second top: the divided by 16 VCO clock
Third top: output signal "up"
Bottom signal: output signal "down"

Figure 4.33 is the zoomed in PDF simulation results which shows either "up" signal or "down" signal keeps high at any time. The entire simulation results show that after the PLL converges or phase locked, both "up" and "down" signals hold steady low which are digital "0" as seen in Figure 4.35.

4.4.1.1.2 Charge Pump and Loop Filter

Figure 4.34 gives the top level schematic circuit of the charge pump and loop filter (second order low pass filter), which implement the integration function.

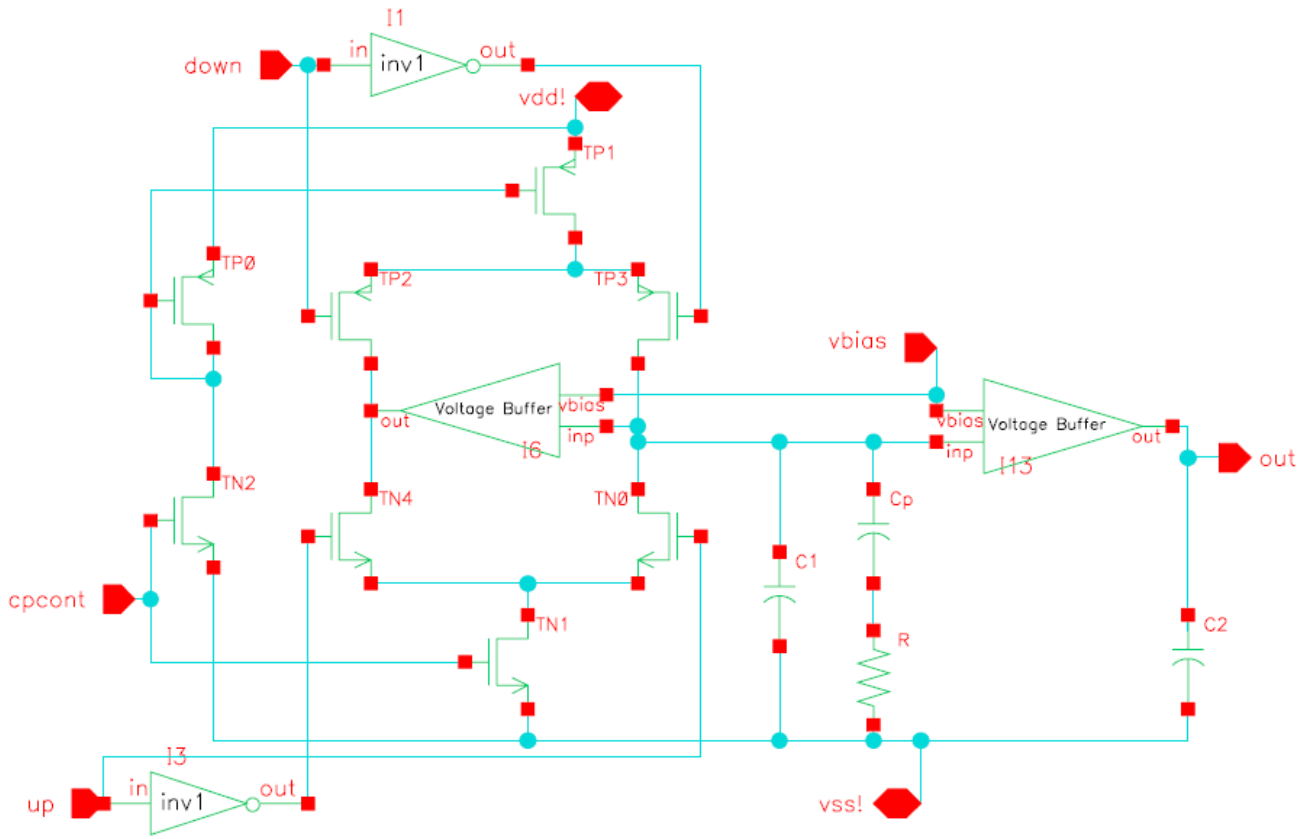

Figure 4.34 Charge Pump and Low Pass Filter Top Level Schematic Circuit

As seen in Figure 4.34, the phase detector controls two current sources (up and down); the loop filter provides the necessary loop dynamics. The basic charge pump circuit is a standard design [110], but some enhancements have been made as will be discussed below. If the phase detector determines the VCO is lagging the input reference, it then activates the bottom current source with "up" high, discharging the capacitor Cp and reducing the analog voltage output of the voltage buffer of I13, so to increase the VCO frequency. If the VCO is ahead, the top current source is activated with "down" high, charging the capacitor Cp and increasing the analog voltage to the VCO, so to decrease the VCO frequency. As shown in Figure 4.34, a minimum gate voltage "cpcont" is provided to the N-channel transistors TN1 and TN2 to ensure TN1, TN2 and TP0, TP1 are always on to reduce the transition time and conserve power consumption. This is in

contrast to the design in [110] where VDD is connected to N-channels and ground is connected to P-channels. This on mode helps to take minimum time to switch on either the up pump or down pump. TP2 and TP3, TN0 and TN4 are differential switches operated by the up and down commands from the phase detector. As discussed in the reference [110], leakage has big effect on the phase noise. Reducing the leakage requires high output impedance. In our charge pump design, the minimum size transistors are used for all the switches, and an analog voltage follower with input high impedance is used as the contributor. The output buffer presents a high impedance to the charge pump and also eliminate the interference between the charge pump and the VCO. Because of the high driving capability of the output buffer, the cascaded transistors which are used in the reference [110] are eliminated. The charge pump and loop filter circuit presented here saved a total of 16 transistors compared to the design in [110].

The main function of the loop filter is to convert the output from the charge pump into a steady voltage proportional to the phase difference between the signals presented at the input of the PFD. The loop filter also has the low pass filter function to help reduce the high frequency transition noise from the switching characteristics of the charge pump. As shown in Figure 4.34, Cp is the charge capacitor with 2.0 pF capacitance; R is added to avoid instability by introducing a zero at $\omega_z = -1/(RCp)$; C1 is parallel to Cp path to form a second order low pass filter. Some relevant calculations are made following the reference [111]. Define ω_n is the natural frequency of the system, which is an indication of the gain-bandwidth product of the loop.

$$\omega_n = \sqrt{\frac{I}{2\pi CpN} K_{VCO}} \tag{4.4}$$

Where I is the averaging charging current which equals to 584 nA in this charge pump design; KVCO is the frequency of the VCO and equals (2π*2GHz)/v in this design; N is the decimation number which equals 2GHz/125MHz=16. So

$$\omega_n = \sqrt{\frac{584\times10^{-9}}{2\pi(2\times10^{-12})\times16}(2\pi\times2\times10^{9})} = 6.04\times10^{6}\,rad/s \qquad (4.5)$$

$$f_n = \frac{\omega_n}{2\pi} = 961\,\mathrm{KHz} \qquad (4.6)$$

ζ is the damping factor which is usually greater than 0.5 and preferably equal to $\sqrt{2}/2$ so as to provide an optimally flat frequency response. R can be calculated by the following equation.

$\zeta = \frac{\omega_n}{2}RCp = \frac{6.04\times10^{6}}{2}R\times2\times10^{-12} = \sqrt{2}/2$. So R is derived to be 117 KΩ.

4.4.2 Schematic Simulation Results of 2 GHz Dual Delay PLL with In phase and Quadrature Output

A PLL with an I/Q dual delay VCO has been designed as shown in Figure 4.31 which is the top schematic level design of Cadence Schematic Editor Tool. The schematic simulation results of the PFD are shown in Figure 4.35 the top two signals which are labeled as “up” and “down”; the DC voltage output of the charge pump and loop filter is labeled as signal “VCO”. The VCO voltage follows the “up” and “down” signals varying until the PLL is locked where the “up” and “down” signal keep stable digital “0”. This indicates the decimated VCO frequency has the same phase or undetectable difference with the reference frequency. The voltage control signal to the VCO holds constant DC value as seen in Figure 4.35, the bottom red signal.

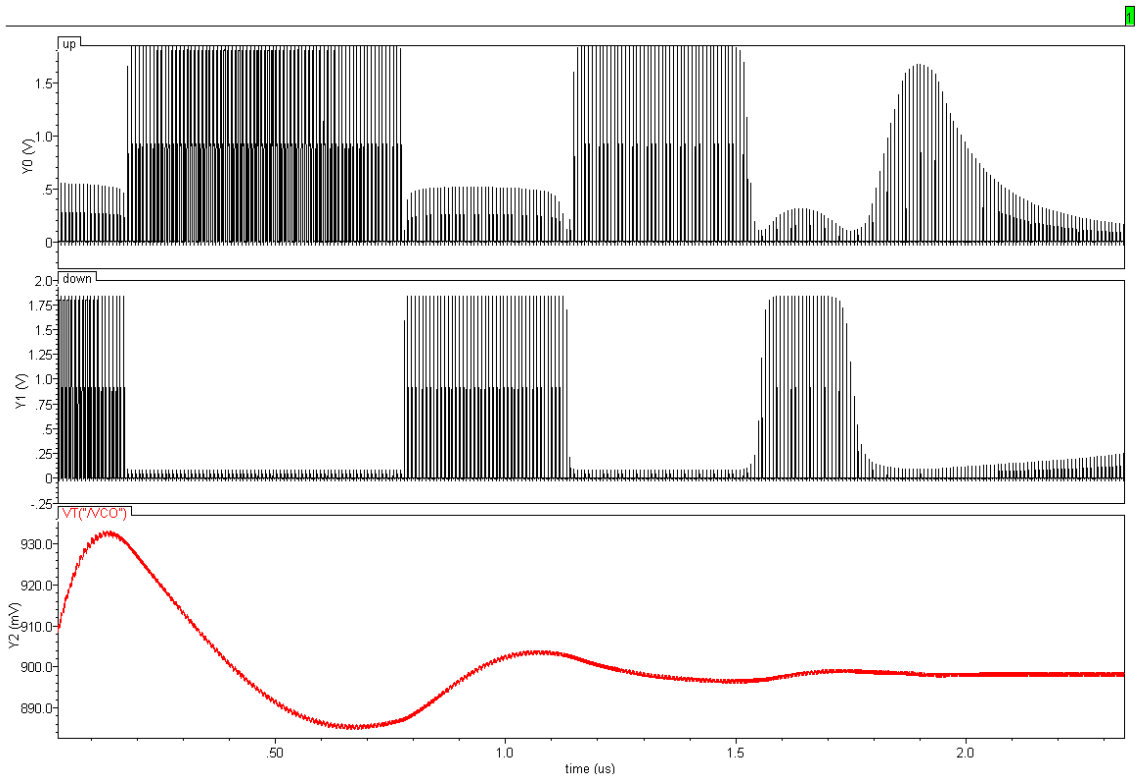

Figure 4.35 I/Q Dual Delay PLL Schematic Simulation Results--Control Signals

Top figure: PLL signal "up"

Middle figure: PLL signal "down"

Bottom figure: charge pump dc voltage output as the input controlled voltage of the dual delay VCO

From Figure 4.35, it can be seen the voltage control input to the VCO is getting steady state as both "up" and "down" signals reach "low". The VCO stable voltage is about 0.9v. The converging time is about 2.1us.

The In phase and Quadrature output which are labeled as out, outb, outQ+, out_Q- are generated as seen in Figure 4.36 and Figure 4.37. Each output has 90 degrees phase shifted compared to its previous one. 'out' and 'outb' outputs are 180 degrees phase difference and 'outQ+' and 'outQ-' output are 180 degrees phase difference too.

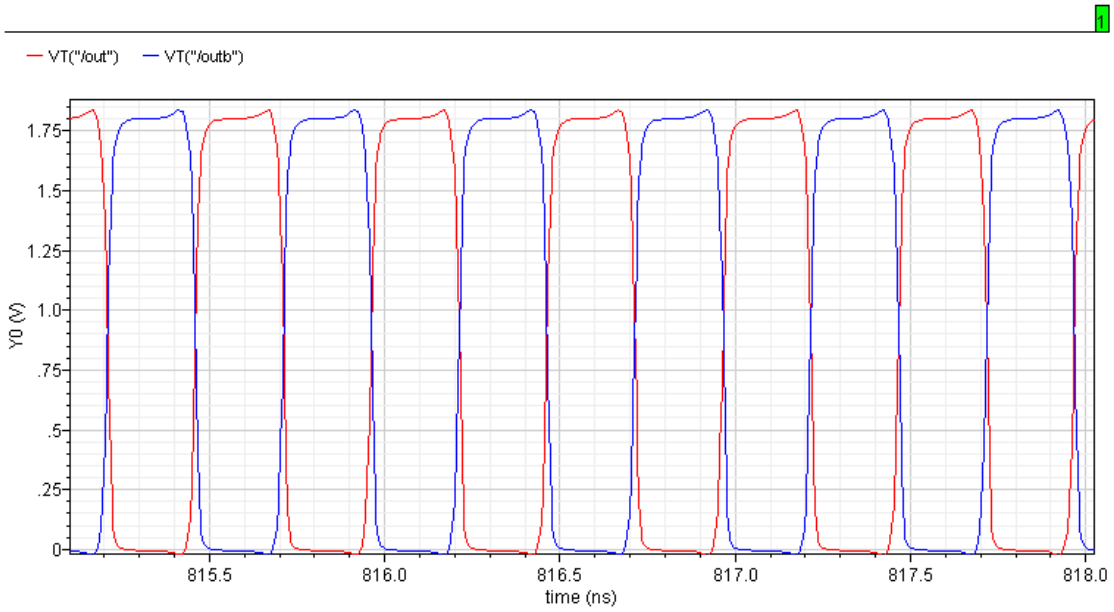

Figure 4.36 I/Q Dual Delay VCO PLL Schematic Simulation Results--out and outb

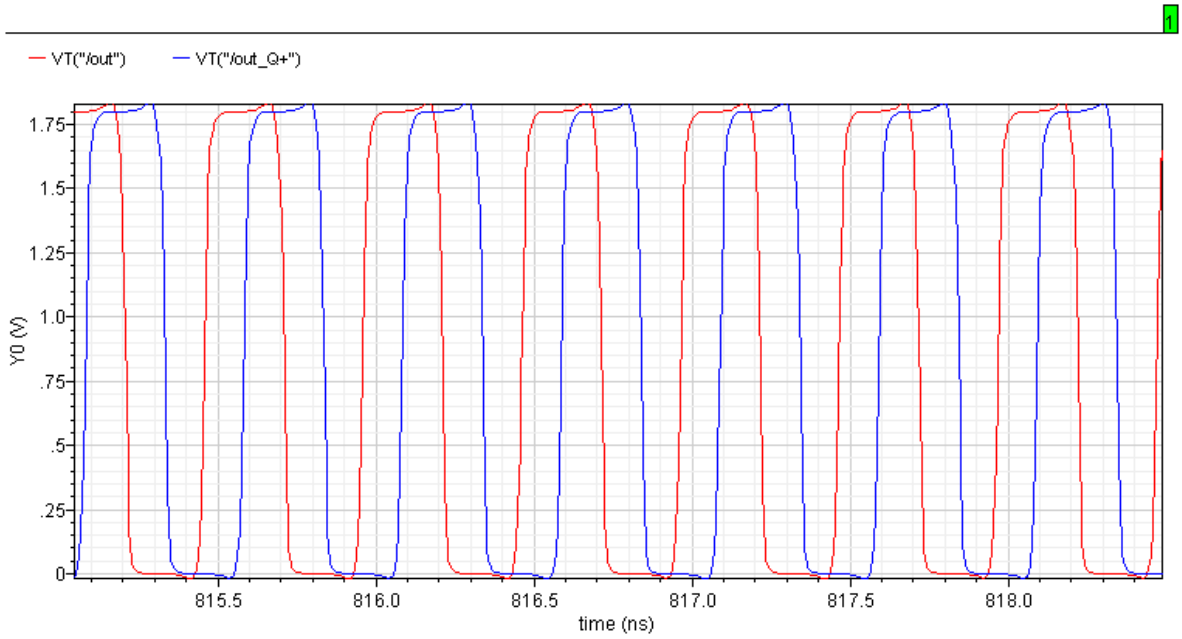

Figure 4.37 I/Q Dual Delay VCO Schematic Simulation Results--out and outQuad

The PLL custom layout is shown in Figure 4.38. The blue and purple rings are the ground and Vdd rails respectively. The right side of the layout is the VCO subsystem. The top right of the layout is the charge pump and loop filter. The middle right is the

phase frequency detector and the bottom right is the clock frequency divider. The total dual delay PLL layout sizes are 200um by 173 um which includes the power supply rails.

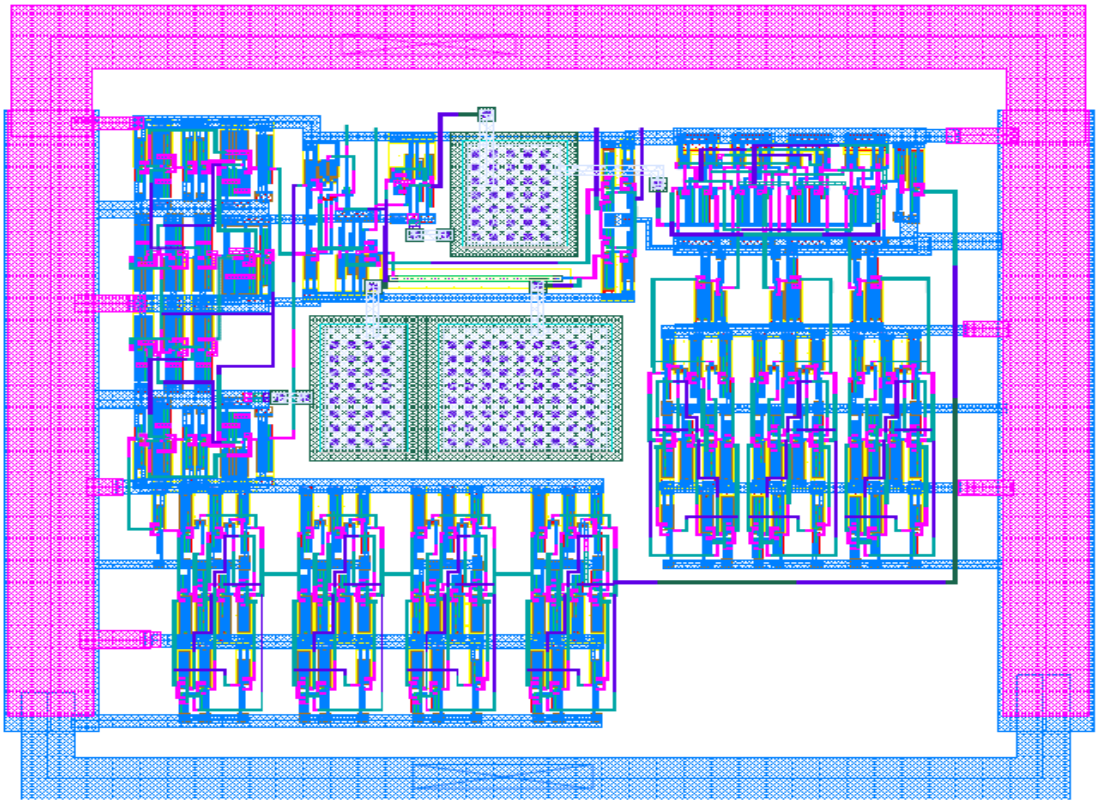

Figure 4.38 I/Q Dual Delay VCO PLL Layout

The layout has been extracted and simulated through Cadence Analog Design Environment. The simulation result indicates that the PLL converges at about 1.3us as shown in Figure 4.39.

Figure 4.40 gives the time domain simulation results which include all the parasitics and potential clock jitters and skews. Figure 4.40 shows that “out” and “outb” signals are 180 degrees out of phase as desired.

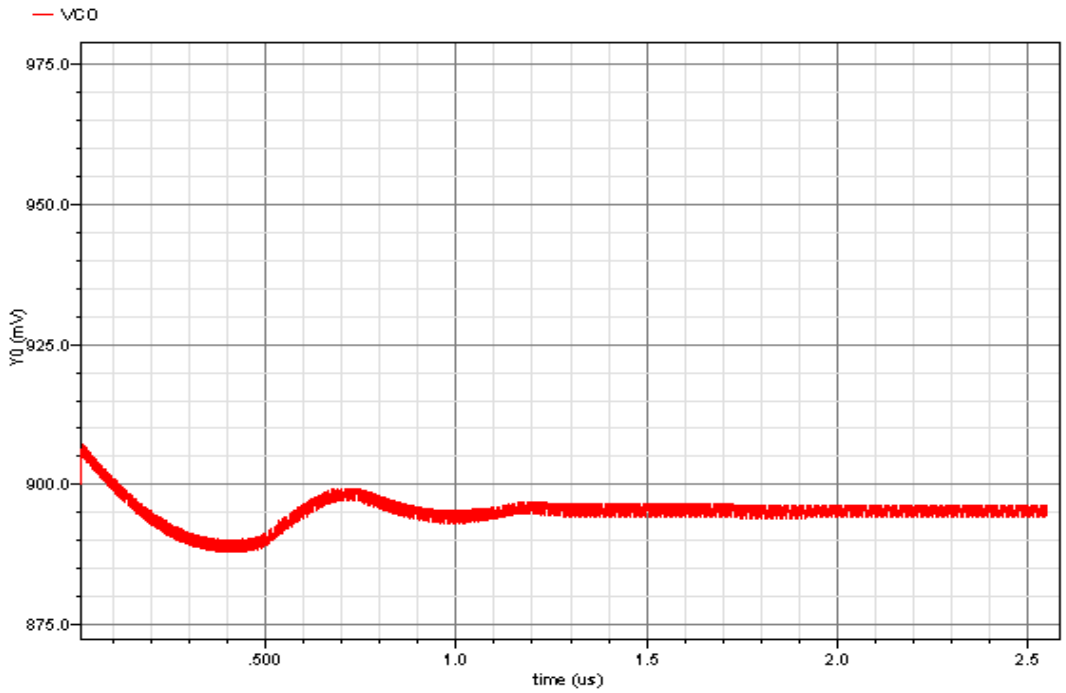

Figure 4.39 PLL Convergence with Dual Delay VCO Layout Results

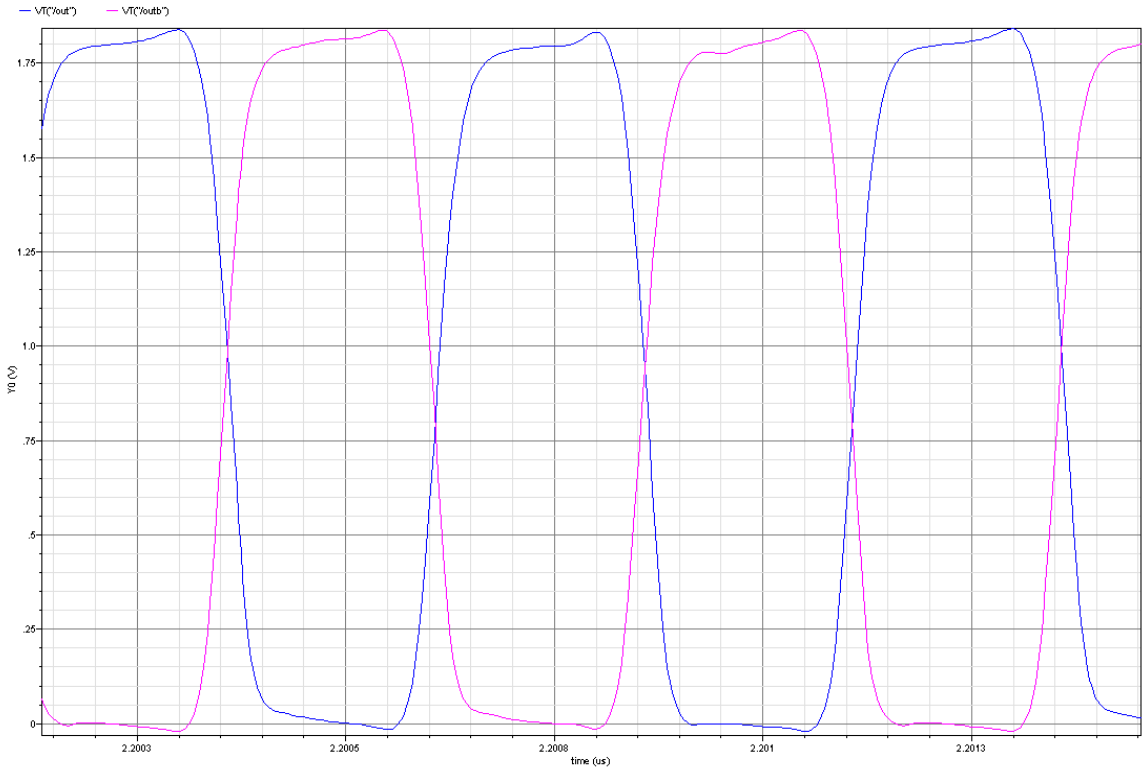

Figure 4.40 PLL with Dual Delay VCO Layout Simulation Results

Figure 4.41 is the FFT result of one of the four quadrature outputs which shows the signal is right at 2.0GHz frequency.

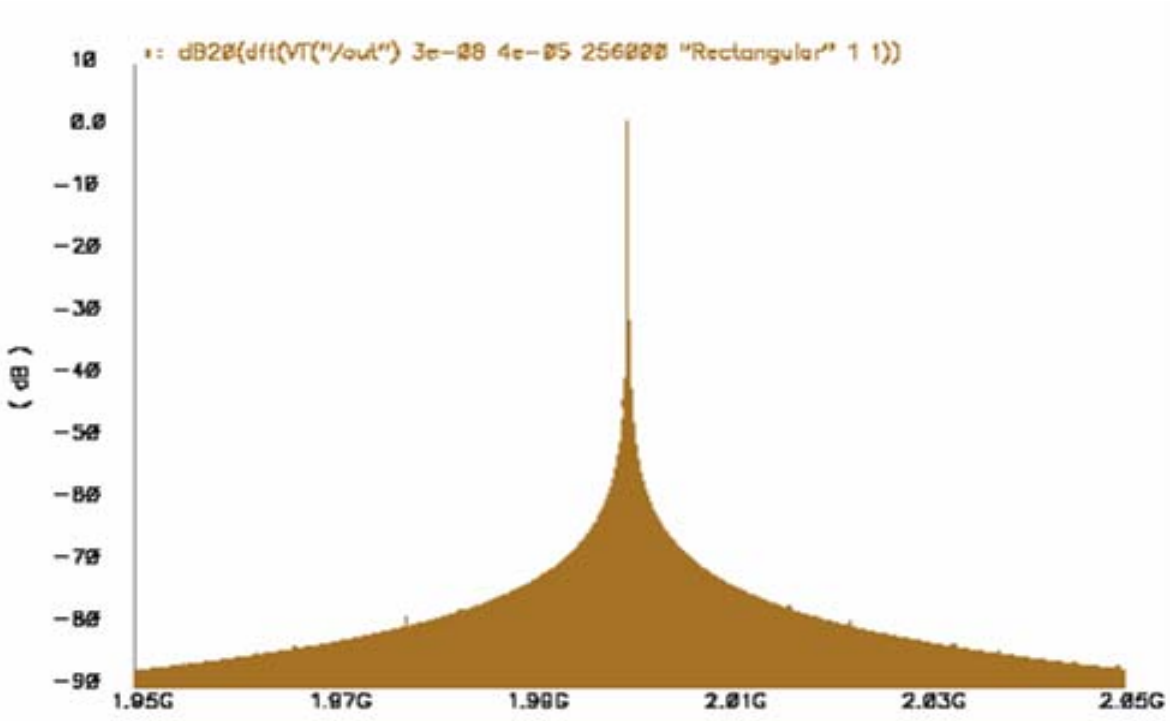

Figure 4.41 FFT Result of PLL with Dual Delay VCO Layout

4.4.3 Prototype Measurement 2 GHz Dual Delay VCO with In phase and Quadrature Output

The above discussed dual delay VCO was taped out through MOSIS and tested. The testing setup is shown in Figure 4.42. The 9 top right wires are ground, Vdd and some other DC biases. The 2 bottom left and 2 bottom right which are total 4 SMA connectors are the four generated quadrature clock signals. The third SMA connector (green cable) of the bottom right is the reference clock input.

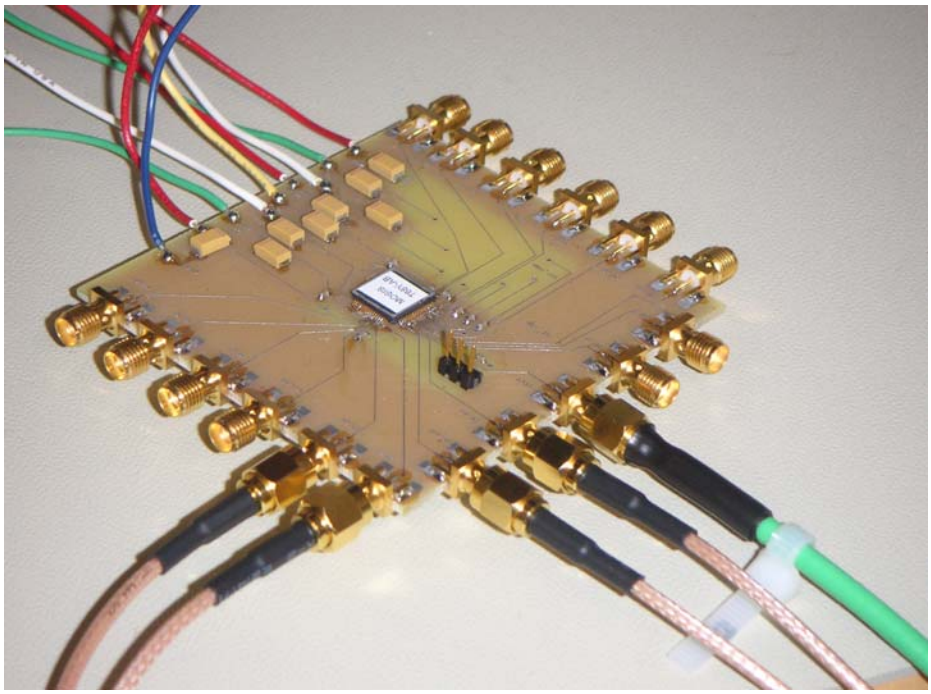

Figure 4.42 2.0 GHz Dual Delay VCO Under Test

Figure 4.43 gives the dual delay VCO measured results for In Phase and Quadrature Outputs at 2 GHz VCO frequency. The circuit was tested using the LeCroy SDA 6000A Serial Data Analyzer with 50 ohm termination impedance and up to 20 GS/s sampling rate. From Figure 4.43 it can be seen the two quadrature output signals are 90^{o} out of phase. The VCO outputs were designed to drive capacitive load instead of 50 ohms resistive load, so the measured results show some attenuation and distortion. Figure 4.44

shows the dual delay VCO tested results for Quad+ and Quad- outputs at 2 GHz frequency with 180 degrees out of phase.

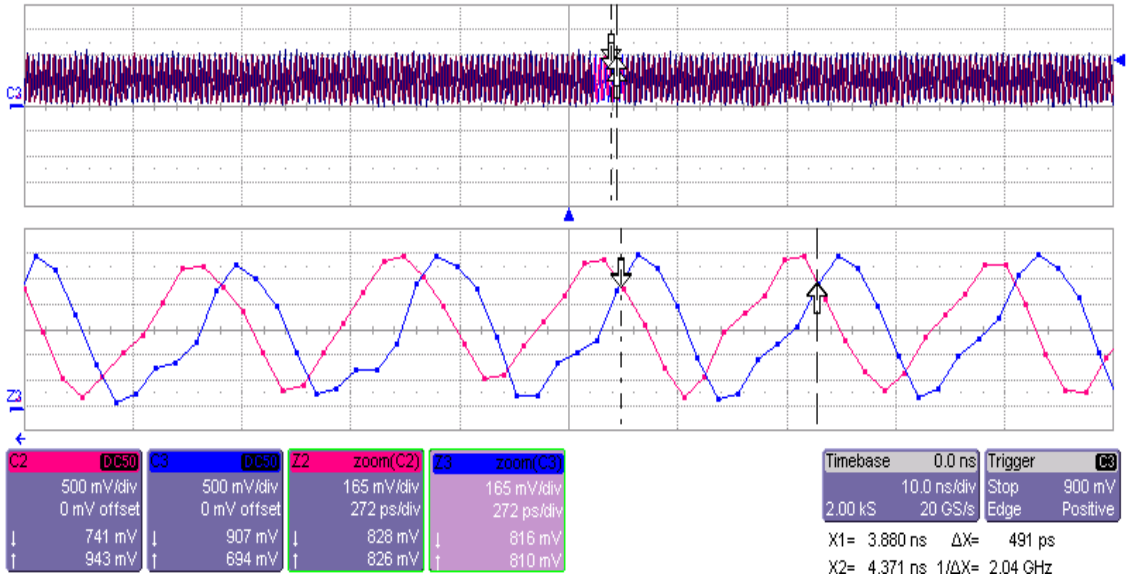

Figure 4.43 I/Q Dual Delay VCO Prototype Tested Results—In Phase and Quadrature

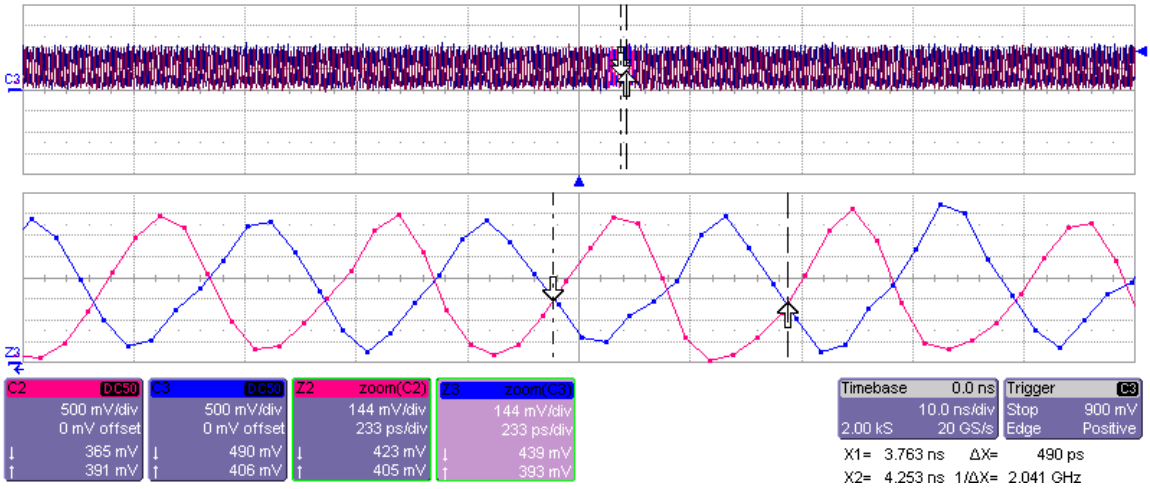

Figure 4.44 I/Q Dual Delay VCO Prototype Tested Results—Two Differential In Phase

As noted above, the VCO outputs are not square waves because the on chip output buffers were not designed to drive the 50 ohm loads. Another source of distortion and phase error is the unequal loading/transmission line paths for the VCO outputs. Since

several subsystems were put on a single die, it was not possible to maintain symmetry on the output transmission line paths. In addition the die pads are wire bonded to the flat pack pins which introduces another source of inductance/capacitance in the signal transmission path. It is also noted that the 20 GS/s sampling time of the scope results in only 10 samples per cycle of the 2 GHz output, so the test results are piece wise connected samples that depend on the sample point. The results confirm functionality of the dual delay VCO at the required frequencies.

The variation of the Dual Delay VCO with control voltage was measured and is shown in Figure 4.45.

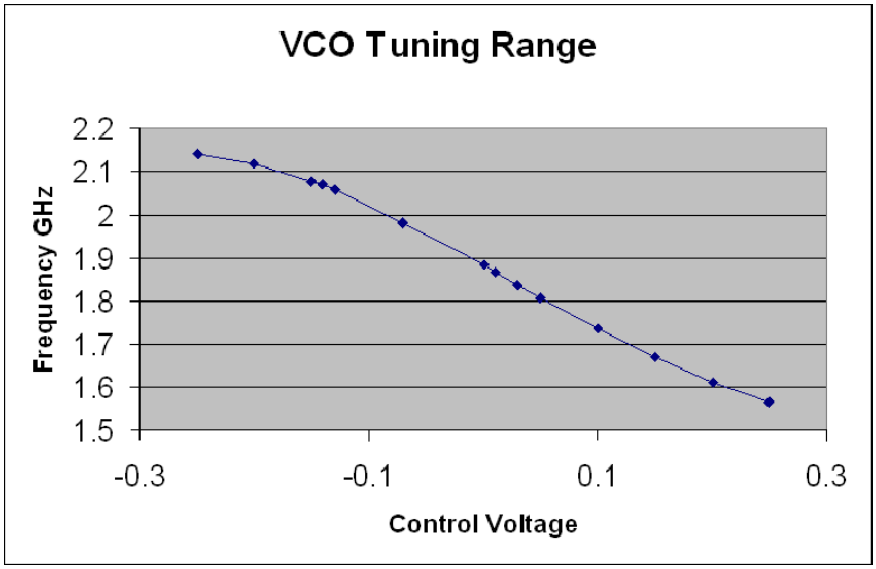

Figure 4.45 Measured Frequency verses Control Voltage Dual Delay VCO

Note that for testing, Vdd is set to 0.9 volts and Vss is set at -0.9 volts to permit inputs with zero offset. The control voltage shown above now varies around 0V rather than 0.9 volts as shown in previous simulations.

Figure 4.46 gives one of the measurements using the Anritsu MS 2721A Spectrum Analyzer. Figure 4.46 shows the Phase Noise is 95.4dbc/Hz at 1 MHz offset and -112.2 dBc/Hz at 5 MHz offset with carrier frequency of 2.0 GHz and 100 KHz resolution

bandwidth. The phase noise should be better if single VCO was fabricated with careful layout to keep every related components, transmission line paths and pads symmetrical. As mentioned above, several subsystems were integrated in a single IC chip to save the fabrication cost. Some of the subsystems share the same power supply, this added extra noise to the tested VCO. For high frequency testing, it usually requires a probe measurement equipment to test the IC pads directly, so to avoid the noise sources from bonding wire and package inductance/capacitance in the signal transmission path.

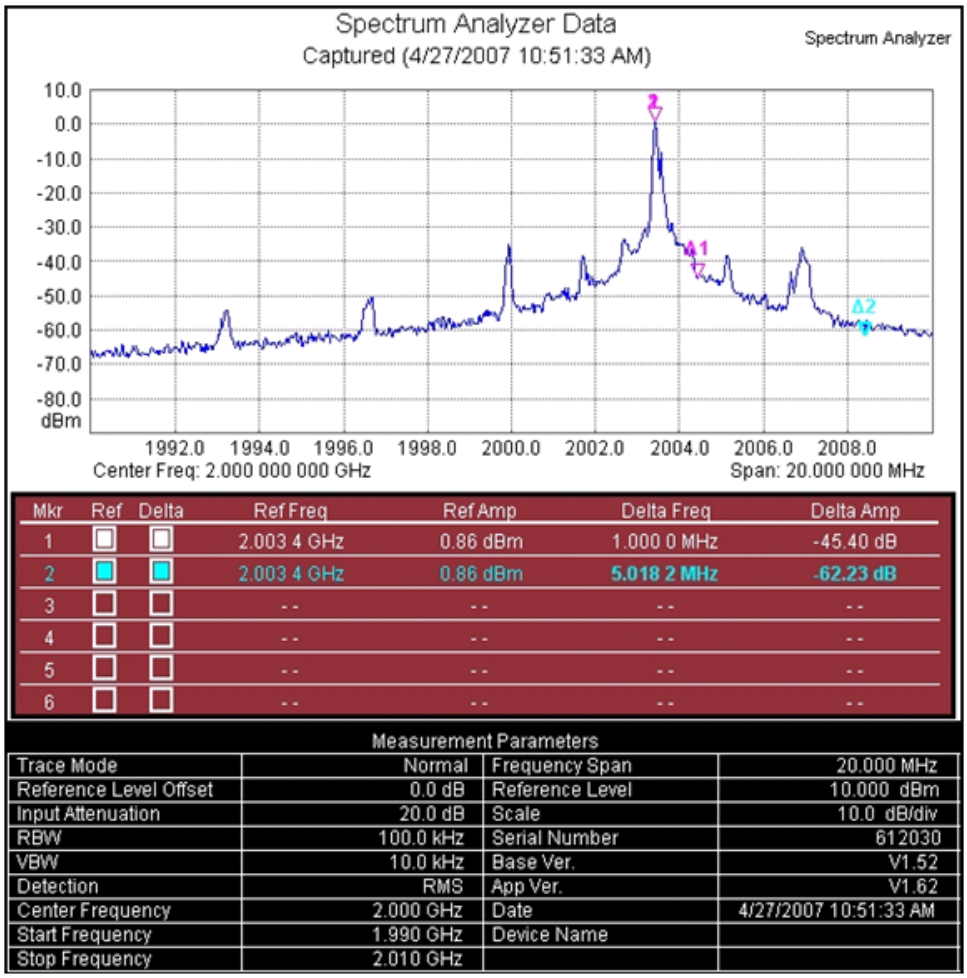

Figure 4.46 Dual Delay VCO Output Spectrum 2.0 GHz Center Frequency

Resolution Bandwidth=100 KHz Input Attenuation=20db
Phase Noise (1 MHz Offset)=-95.4dbc/Hz

Phase Noise (5 MHz Offset)=-112.2dbc/Hz

4.5 Time Interleaved Delay-Locked Loop Clock Generator

Another frequency synthesizer effort was focused on the delay locked loop clock generator circuit for realizing the precise time interleaved clocks that are required for a time interleaved ADC applications such as the four channels of the Parallel Time Interleaved Band Pass ADC. The clock signals going to each of the time interleaved channels are 800 MHz signals, but each must be delayed with respect to the previous clock in the sequence by a time of 312.5 ps (1/3.2 GHz). The clock generator circuit incorporates a Delay-Locked Loop to help synchronize the four time interleaved clock signals. A block diagram of this circuit is shown in Figure 4.47 below.

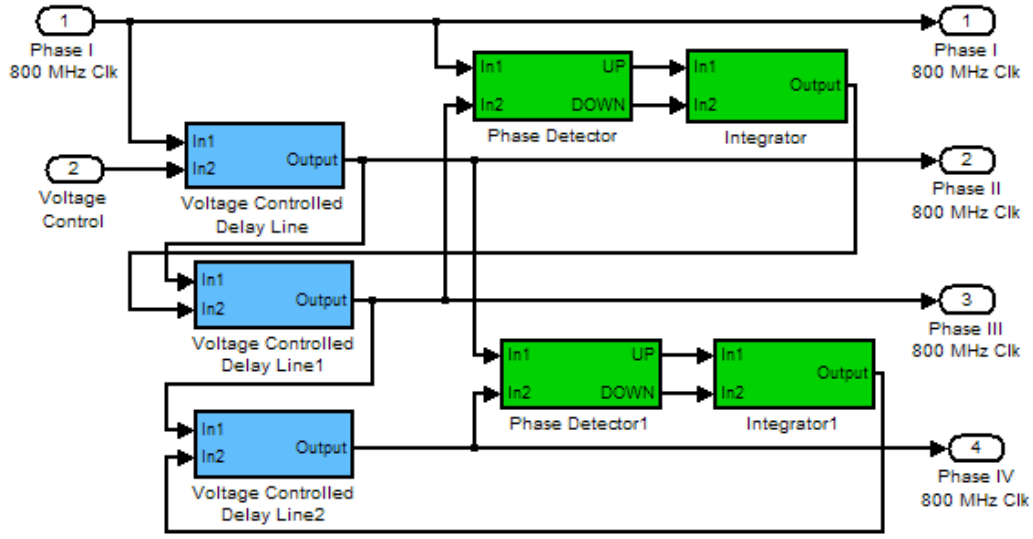

Figure 4.47 Block Diagram
Time Interleaved Delay-Locked Loop Clock Generator

As seen in Figure 4.47, the Phase I clock is obtained from either an off chip or on chip oscillator. A combination of voltage controlled delay lines, phase detectors, and integrators are used to generate the other three phases so that each phase has the proper

delay with respect to the others. The voltage controlled delays are nominally set for 312.5 ps delays from the input clock signal to the output clock signal; however this delay can be adjusted based upon the voltage control input. The schematic of the Voltage Controlled Delay Lines (VCDL) as captured in the Cadence Virtuso Schematic Composer Tool is shown in Figure 4.48 below.

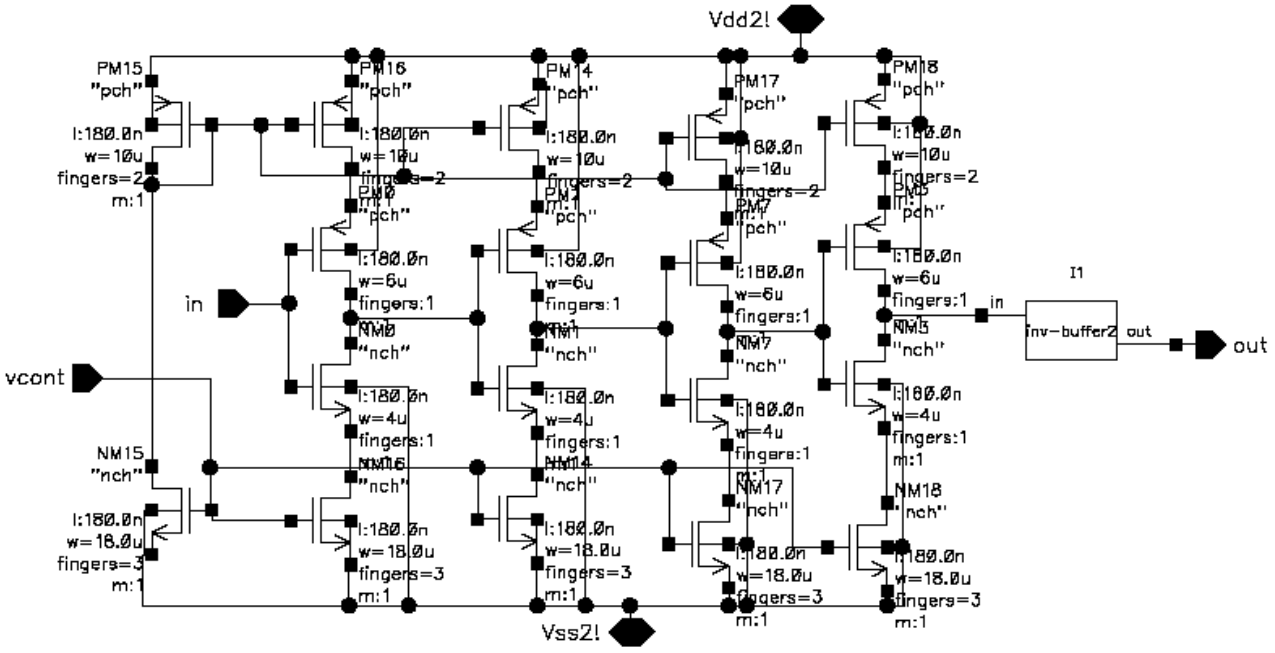

Figure 4.48 Voltage Controlled Delay Line (VCDL)

As seen in Figure 4.48, the VCDL is based upon a cascade of current controlled inverters. The current available to each inverter is controlled by the voltage control input, so that the effective delay from input to output can be varied. The circuit has been designed to have a delay of 312.5 ps with a voltage control input of 0.7 volts. The delay can be varied from 218 ps to 426 ps with the voltage control changing from 0.6 to 0.8 volts. Again referring to Figure 4.47, it is seen that a Phase Detector is used to determine the relative phase of the Phase I clock and the Phase III clock. When Phase I has an edge

that is going from low to high, Phase III should have an edge that is going high to low, since the two clocks are 180 degrees out of phase. The phase detector determines which edge leads and generates a small up or down signal to an integrator for providing a feedback voltage control signal to the VCDL. The schematic of the Phase Detector is shown in Figure 4.49.

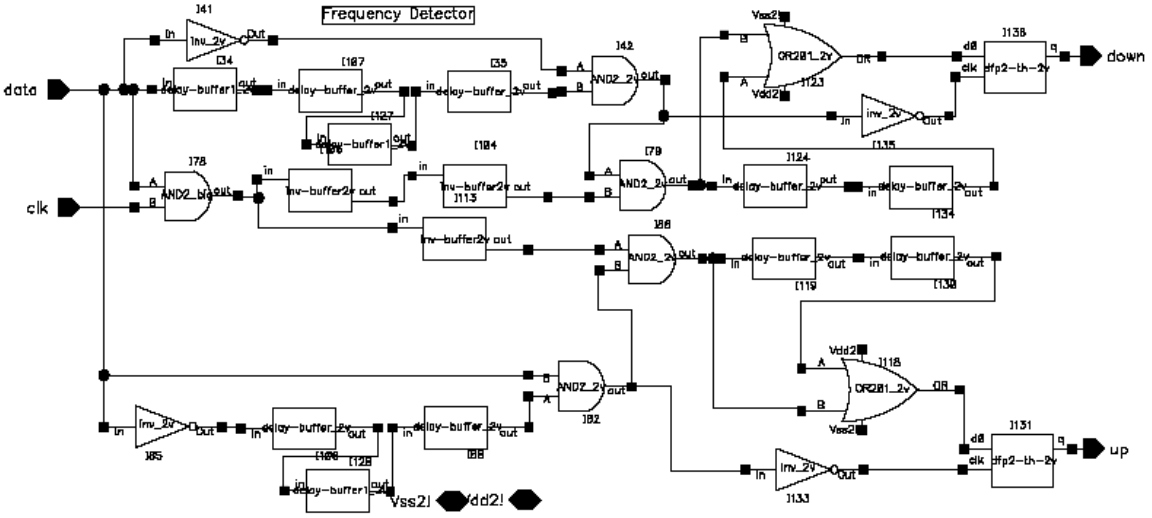

Figure 4.49 Phase Detector

The phase detector has been designed to detect the rising edge of the Phase I clock and the falling edge of the phase III clock and determine which one leads the other. The feedback circuit slowly adjusts the voltage control to the VCDL until the edges of the two clocks are in phase. In a similar manner a second Phase Detector determines the relative phase of the Phase II clock and the Phase IV clock, which are also 180 degrees out of phase. A feedback circuit adjusts the voltage control to the VCDL so that the rising edge of the Phase II clock is in phase with the falling edge of the Phase IV clock. The schematic of the Time Interleaved Delay-Locked Loop Clock Generator as captured in the Cadence Virtuso Schematic Composer is shown in Figure 4.50 below.

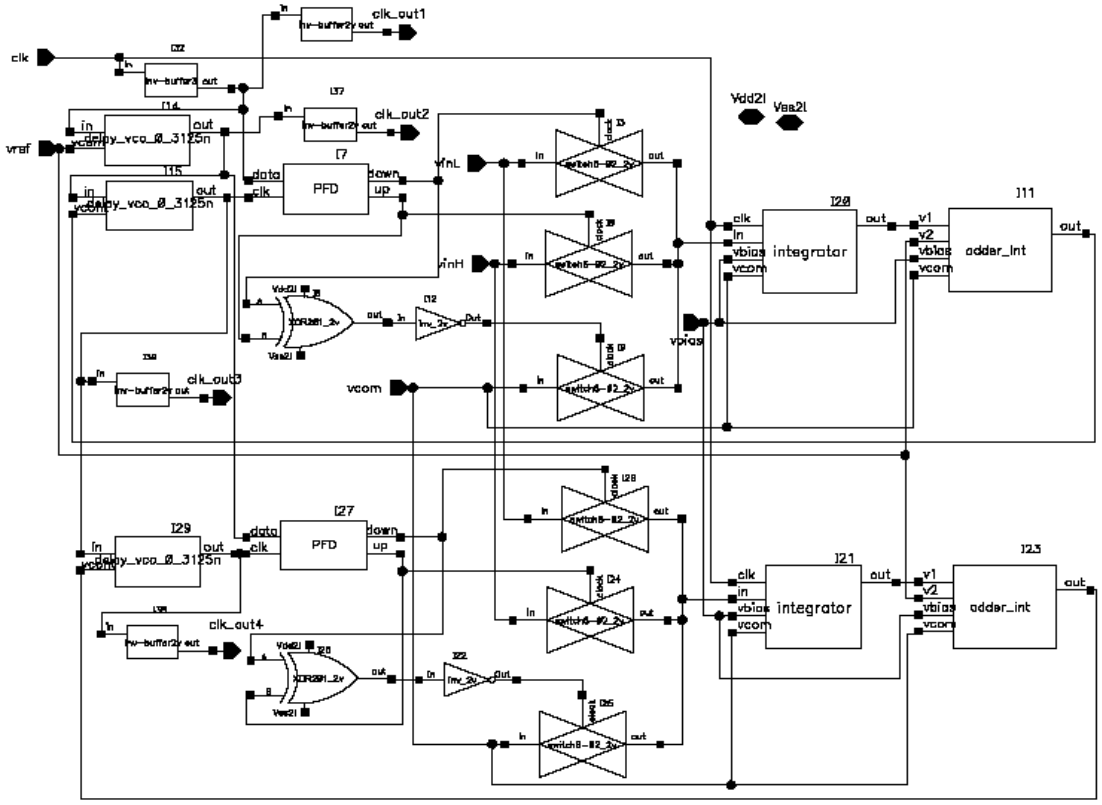

Figure 4.50 Schematic Diagram
Time Interleaved Delay-Locked Loop Clock Generator

Simulations were performed based upon the net lists extracted from Figure 4.50 to demonstrate the functioning of the Time Interleaved Delay-Locked Loop Clock Generator. For the simulation, a fairly large clock skew was introduced between the Phase I and Phase III clocks (~60ps). As seen in Figure 4.51 below, the feedback voltage to the VCDL is adjusted downward until the rising edge of the phase I clock is in phase with the falling edge of the Phase III clock. Then the feedback voltage oscillates about the steady state value to maintain the clock phases. The simulation outputs of the Phase I and Phase III clocks are shown in Figure 4.52. It is noted that the two clocks are not phased properly at the beginning (~60ps skew), but the phases are adjusted by the Delay-Locked Loop circuit.

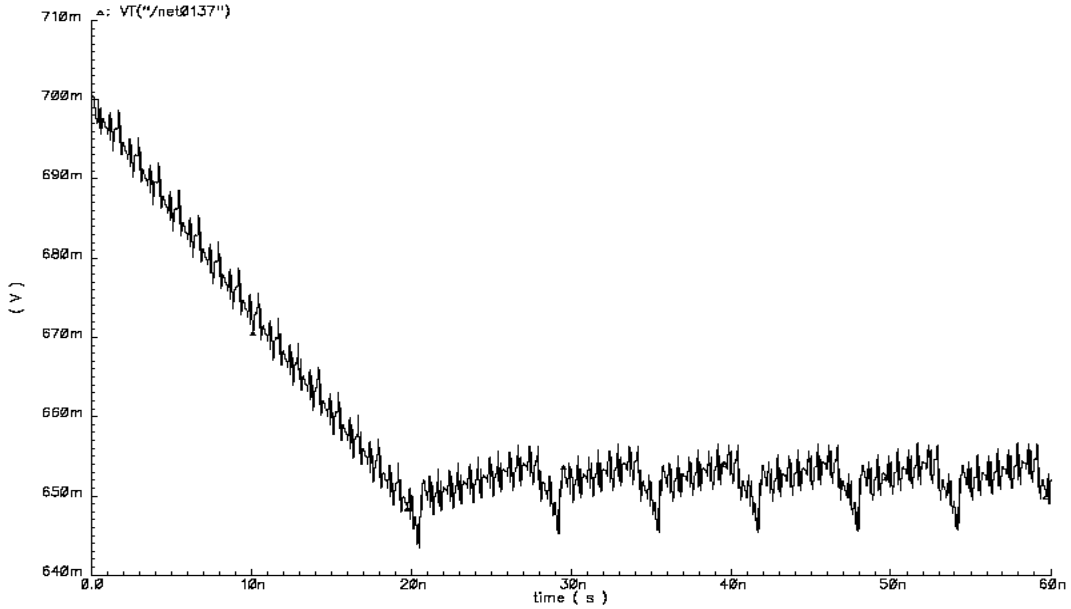

Figure 4.51 Feedback Voltage to VCDL

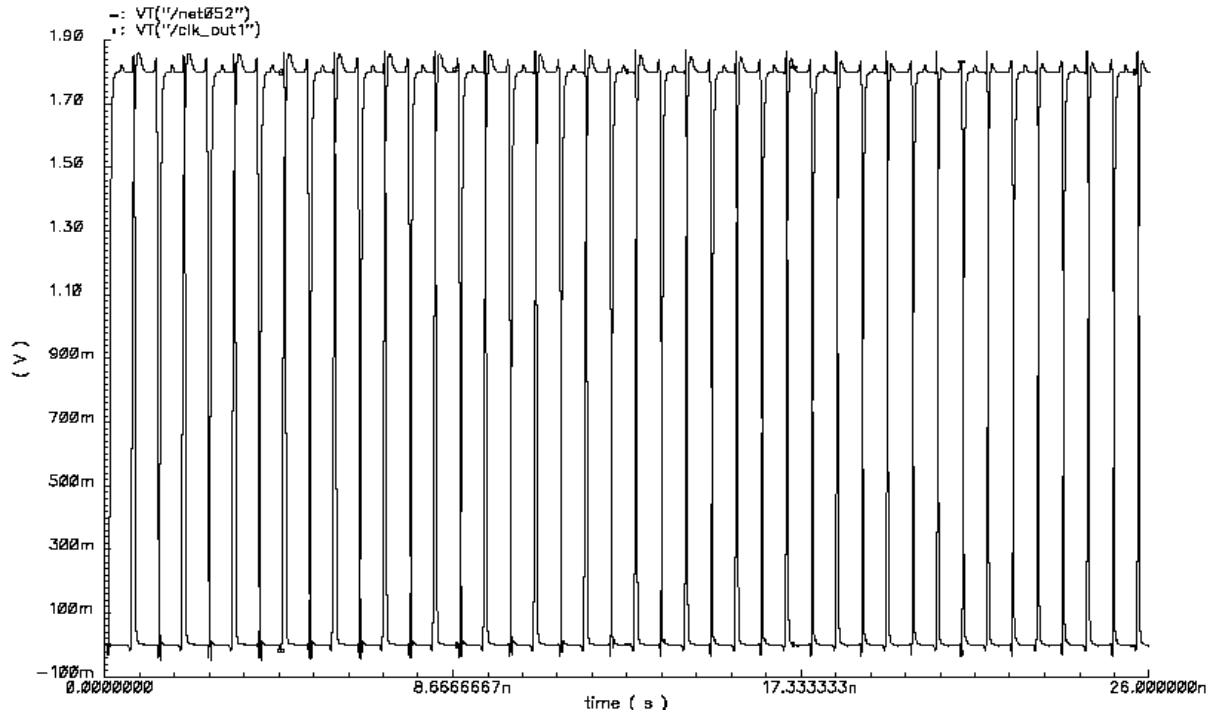

Figure 4.52 Phase I and Phase III Clocks

4.6 Conclusion

This chapter has presented several on chip clock generator architectures which includes a wide range transconductor based VCO, dual delay VCO, phase locked loop with dual delay VCO and delay locked loop VCO.

The schematic simulation results show that the wide range transconductor based VCO oscillating frequency can go as high as 4.1 GHz with 3.1 mW power dissipation; and the minimum oscillating frequency approaches DC. One specific prototype measurement shows the oscillating frequency covers the range 4MHz to 1.0GHz. The measured range was limited by the equipment that was available. Table 4.3 gives the performance summary of the transconductor based wide range VCO, the I/Q dual delay VCO presented here and reported state of the art VCOs. It can be seen the presented transconductor based VCO has a very wide tuning range, full scale dynamic range and relatively low power dissipation with differential output feature, but the phase noise is relatively high. The wide range VCO was designed to support our requirement for an on chip ADC clock source for prototype testing, so the wide tuning range was obtained with sacrifice of increased phase noise.

The Dual Delay VCO produces a clock source with precise quadrature outputs which can be used in time interleaved ADCs, and receiver mixers, among other applications. Compared with transconduator based VCO, the tuning range of the dual delay VCO is narrower, but still has a range of hundreds of MHz. The phase noise could be smaller if some addition design effect was made [104]. The results indicate that it is easier to get higher oscillating frequency than low oscillating for the dual delay VCO. A further development dual delay VCO design shows that the oscillating frequency can reach

7.8GHz with IBM 0.18um technology. It would be possible to have a CMOS VCO in 10 GHz oscillating frequency region if CMOS technologies with smaller feature size were used (130nm, 90nm, even 65nm).

The delay phased locked loop is another alternative for TI ADC application. It shows the delay of each block does not quite match, even with the same layout design and same DC input control. For a low frequency application, this is acceptable, but for higher frequency applications it will need more study.

Table 4.3 Performance Summary of the Proposed VCOs and State of the Art VCOs

Design	This Design		[112]	[113]	[114]	[115]
Technology (CMOS)	0.18μm		0.18μm	0.18μm	0.13μm	0.35μm
Supply Voltage	1.8v		1.8v	2v	1.2v	3.0v
	Wide Range VCO	Dual Delay VCO				
f_0 (GHz)	2.0	2.0	1.81/5.79	5.0	5.0	1.8
Output Type	Differential	Quadrature	Three/Nine	Differential	Single	Quad
Tuning Range Percentage	161%	36.3%	42%/ 13.3%	36%	24%	11.1%
Phase Noise @1MHz (dBc/Hz)	-93	-95.4	-105/ -99.5	-85	-120	-105 @ 100KHz Offset
Power	3.1mW	8.1mW	N/A	80mW	24mW	60mW

5 Conclusions and Future Work

5.1 Conclusions

This research has focused on making a contribution to the field of analog to digital conversion with emphasis on ADC architectures and on chip clock generation techniques that can be implemented with advanced CMOS integrated circuit technology.

5.1.1 ADC Architectures

Two new ADC architectures are developed in this research.

5.1.1.1 Pipelined Delta Sigma Modulator (PDSM) ADC

This architecture uniquely combines delta sigma modulation with pipelining using a new residue averaging technique and is aimed at applications requiring both broad bandwidth and high resolution [48, 49, 116, 63, 66, 91, 72, 117]. The research includes the complete development of this architecture from architecture definition, MATLAB SIMULINK model development and analysis to verify potential performance advantages over existing architectures, complete schematic circuit design and layout design using 180 nm CMOS technology with simulation results, fabrication of prototype circuits, test fixture design, and testing of the fabricated prototype.

Some key features of the PDSM ADC architecture are:

- High resolution and broad band operation with low OSR
- Accuracy requirements for track and hold circuits, analog subtract circuits, and DAC are mitigated by the analog averaging of the error signal

- Over all component matching and accuracy requirements are reduced by the over sampling delta sigma configuration
- Nonlinearity of the first stage DAC/quantizer is included in the error signal and the effect of the nonlinearity is reduced when the second stage output is combined with first stage output
- Pipeline operation is based on first stage generating 6-7 most significant bits and second stage generating 5-6 least significant bits using first order delta sigma modulators.
- PDSM architecture differs from MASH or feed forward architectures that seek to obtain higher order delta sigma operation. First order modulators used by PDSM ADC facilitate high sampling rates.

MATLAB simulation and FFT results were presented for the two stage PDSM ADC using sampling frequency of 1.0 GHz and an input bandwidth of 62.5 MHz. The MATLAB results support 13-15 bit resolution over the 62.5 MHz bandwidth. A transistor level 0.18um CMOS version of the design was captured using Cadence design tools with modulators and other components that can be clocked at 1 GHz. The FFT results, based on simulations of the CMOS 0.18um design, show 12 bit resolution with a 50 MHz input. The fabricated prototype measurements for first stage PDSM ADC show a resolution of 6-8 bits per stage as predicated by analysis and simulation. These results support the practicality of using the PDSM ADC for applications where there is a need for high resolution and broad band operation.

5.1.1.2 Time Interleaved Band Pass Delta Sigma Modulator ADC

This unique architecture is defined and developed to support applications requiring band pass ADCs at RF and IF center frequencies [96, 92]. The unique advantages of this ADC architecture are developed based on MATLAB/SIMULINK models and analysis.

The Simulink/Matlab simulation results show the following features of this TI DSM BPADC.

- The results presented for the TI Delta Sigma Band Pass ADC show that the architecture supports flexible IF center frequencies without changes in hardware.
- Center frequencies are modified by changing the clock frequency of the modulator, low pass filter and multiplexer.
- The resolution is determined by the modulator clock frequency and the bandwidth of the low pass (band pass) filters. The resulting bandwidth (fb) of the band pass ADC is twice that of the low pass filter centered at either fs (first Nyquist region) or 3fs (second Nyquist region).
- More resolution is obtained if the ratio of fs/fb is increased.
- The multi-channel receiver architecture was used as an example and demonstrated the flexibility of the TI Delta Sigma Band Pass ADC.
- The TI Delta Sigma Band Pass ADC allows a tradeoff between bandwidth and resolution. For resolutions of above 8 bits application, the ration of 4fs/fb must be larger than 10.
- An alternative configuration for the TI Delta Sigma BPADC was defined that used only a single band pass filter, rather than a low pass filter in each channel.

The performance for the two configurations was about the same. The single band pass filter may save some hardware, but it must be clocked at 4*fs rather than fs.

- A Pipelined Delta Sigma Modulator (PDSM) ADC can be used in place of the Low Pass Delta Sigma Modulator to increase resolution for a given over sampling ratio. The resolution is increased with the cost of additional hardware and complexity.

In summary the combination of time interleaving with delta sigma modulation results in relatively high RF/IF center frequencies and good resolution with relatively low component clock frequencies. Sampling frequencies for the track/hold, modulators and low pass filters of less than 1 GHz support RF center frequencies up to 3 GHz. The relatively low sample rates facilitate an ASIC implementation in CMOS technology.

5.1.2 On Chip Clock Generation Techniques for ADC Applications

Four on chip clock generator circuits are developed which have unique capabilities for CMOS ADCs and receiver/transmitter applications.

5.1.2.1 Wide Range Voltage Controlled Oscillator (VCO)

A wide range VCO architecture is developed including schematic and layout design in 180 nm CMOS technology together with fabrication and test results [118]. This custom IC facilitates an on chip clock generator with frequency ranges of over 1 GHz, low power dissipation, and differential outputs.

The schematic simulation results show that the wide range transconductor based VCO oscillating frequency can go as high as 4.1 GHz with 3.1 mW power dissipation; and the minimum oscillating frequency approaches DC. One specific prototype measurement

shows the oscillating frequency covers the range 4MHz to 1.0GHz. The measured range was limited by the equipment that was available. Comparing to the state of the art on chip VCOs, it is seen the wide range transconductor based VCO has a very wide tuning range, full scale dynamic range and relatively low power dissipation with differential output feature. The phase noise is relatively high, which is tradeoff for the wide tuning range. The wide range VCO support our requirement flexibility in testing ADCs as well as applications requiring a wide range of on chip local oscillator frequencies.

5.1.2.2 Dual Delay VCO

A dual delay VCO is developed which features precise In Phase and Quadrature outputs for applications that require I/Q clocks, such as time interleaved ADCs and mixers. The dual delay VCO is designed in CMOS 180 nm technology, fabricated and tested as part of this research.

Comparing with a wide range transconduator based VCO, the tuning range of the dual delay VCO is narrower, but is sufficient for many applications. The architecture has potential low phase noise by combining some additional design features. The results indicate that it is easier to get higher oscillating frequency than low oscillating frequency for the dual delay VCO. A further development dual delay VCO design shows that the oscillating frequency can reach up to 7.8GHz with IBM 0.18um CMOS technology. It would be possible to have a CMOS VCO in 10 GHz oscillating frequency region if CMOS advanced technologies with smaller feature size were used, such as 130nm, 90nm, even 65nm technologies.

5.1.2.3 Phase Locked Loop with Dual Delay VCO

A Phase Locked Loop is developed using the dual delay VCO including schematic and layout design in 180 nm technology and fabrication with test results. The PLL architecture includes a highly stable off chip reference clock in a feedback loop to reduce the clock jitter and phase noise. Test results demonstrated low power operation at 2 GHz frequency with very good phase noise [119].

5.1.2.4 Delay Locked Loop

A delay locked loop is developed with 180 nm CMOS technology to meet the requirement for on chip clock generation for time interleaved ADC applications. Simulations supported good performance at relatively low frequencies (up to 800 MHz), but there were issues such as absence of 50% duty cycle at higher frequencies.

5.2 Future Work

5.2.1 Low Pass Pipelined Delta Sigma Modulator ADC

5.2.1.1 Additional Effort to Plan Testing of Fabricated Circuits

As discussed in Chapter 2, the PDSM ADC architecture has potential for 13-15 bits of resolution with 7-8 bits from the first stage and 6-7 bits from the second stage based on simulations of the schematic and layout designs. However test results did not indicate the expected gain in resolution from the second stage. A critical circuit is the circuit between stages that generates the analog error residue. This residue signal must be accurate to the desired resolution of the final two stage signal. The circuitry includes an analog subtract circuit that forms the difference between the first stage digital output after converting to

analog and the delayed analog input, an analog multiplier circuit, an analog SINC filter, and second analog multiplier. Simulations indicated that these circuits operated with the required accuracy, but the fabricated test results did not support the simulations. For testing circuits at high frequencies, the design of the test fixture becomes as critical as the circuit under test. The analog circuits that generate the residue signal require power supply inputs that can source and sink the required currents at high frequencies while not generating noise and ground bounce that effect the performance of the circuits. For future work, where testing is to be done for high resolution circuits, additional effort should be made in designing and fabricating the test circuits. Particular focus should be placed on the design of the residue generation circuits together with a test fixture that will not degrade performance when under test.

5.2.1.2 Calibration Techniques

Obtaining resolution in the 10-15 bit range usually requires some type of calibration mechanism as part of the ADC design. The PDSM ADC architecture could be analyzed with the objective of adding appropriate calibration circuitry.

5.2.2 Flexible RF/IF Band Pass ADC

The results presented in this research were based on MATLAB/SIMULINK models and simulation. Future work could concentrate on circuit level designs and simulations with possible fabrication and testing.

5.2.3 On Chip Clock Generators

The Wide Range VCO provides flexibility in generation of on chip clocks with a wide frequency range. This VCO could be integrated as part of PLL to obtain a frequency

synthesizer with reduced phase noise and a wide range of output signals. A single PLL base frequency synthesizer could be used for applications required multiple on chip clock frequencies.

The Dual Delay VCO/Phase Lock Loop clock generation provides stable on chip clocks with I/Q outputs. Future efforts could be aimed at reducing phase noise by investigating LC Tank based VCOs using a similar architecture.

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